FACULTY OF INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING
DEGREE PROGRAMME IN ELECTRONICS AND COMMUNICATIONS ENGINEERING

MASTER'S THESIS

DESIGN OF ANALOG PREDISTORTER

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ABSTRACT

In this thesis, two analog predistorter circuits are designed for linearizing the CMOS power amplifier in MIMO transceivers. The first circuit uses two parallel transistors as conventional derivative superposition, where derivatives of the transistor drain currents are biased to have opposite phases for 3rd-order distortion components. This results in the cancellation and thus providing a very linear 3rd-order response. The other design, using complementary derivative superposition topology, has p- and n-type transistors with a common drain self-biasing to achieve expansive power gain. This is used to improve the 1-dB compression point of the CMOS power amplifier.

Simulation results of conventional derivative superposition circuit show over 25 dB improvement in distortion level, while still providing a fair amount of power gain. Implementation with a CMOS power amplifier shows a 2.6 dB improvement in 1 dB compression point. With the circuit having expansive characteristics, adjustable gain-expansion behaviour is achieved. With the implemented digital bias control, expansion between 2.5 dB and 4 dB is achieved, with gain variation between -2.4 dB and 1 dB. With a CMOS power amplifier, 3.5 dB improvement in 1 dB compression point is achieved, allowing the power amplifier to be used with greater efficiency. Both circuits are implemented using 22nm CMOS SOI technology and submitted to fabrication.

Keywords: power amplifier, millimetre wave, circuit design, linearization, superposition.

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TIIVISTELMÄ

Tämän diplomityön tavoitteena on suunnitella kaksi erilaista analogista esisärötinpiiriä, joita voidaan käyttää laajakaistaisten radiotaajuisten lähettimien linearisoinnissa. Työssä esisärötinpiirien avulla linearisoidaan pienitehoinen integroitu RF tehovahvistin. Toinen piireistä perustuu kahden rinnakkaisen transistorin superpositioperiaatteeseen, jossa transistoreiden nieluvirtojen derivaatat sovitetaan siten, että niiden kolmannen asteen särökomponentit ovat vastakkaisvaiheiset. Tämä aiheuttaa vastakkaisvaiheisten komponenttien kumoutumisen, jolla saavutetaan erittäin lineaarinen kolmannen asteen vaste. Toisessa piirissä, joka käyttää päällekkäistä superpositiorakennetta, p- ja n-tyypin transistoreiden nielun itsebiasoinnilla saadaan aikaan ekspansioiva tehovahvistus. Tätä käytetään parantamaan RF-tehovahvistimen yhden desibelin kompressiopistettä.

Simuloimalla rinnakkaista superpositiopiirirakennetta, saavutetaan yli 25 desibelin parannus kolmannen kertaluvun keskeismodulaatiosäröön. Samalla saadaan kohtuullinen määrä tehovahvistusta. CMOS-tehovahvistimen kanssa, piiri parantaa 2.6 desibeliä tehovahvistimen yhden desibelin kompressiopistettä. Ekspansioivalla piirirakenteella saadaan toteutettua helposti säädettävä vahvistus-ekspansio suhde. Implementoidulla digitaalisella biasohjauksella saavutetaan ekspansiota 2,5 desibelistä 4 desibeliin, samaan aikaan vahvistuksen vaihdellessa -2,4 desibelistä 1 desibeliin. Linearisoinnilla CMOS-tehovahvistimen 1 desibelin kompressiopistettä saadaan kasvatettua 3,3 desibeliä, minkä ansiosta tehovahvistinta voidaan käyttää paremmalla hyötysuhteella. Molemmat piirit toteutetaan 22nm CMOS SOI -teknologialla ja ne toimitetaan valmistukseen.

Avainsanat: Tehovahvistin, millimetriaalto, piirisuunnittelu, linearisointi, superpositio.

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FOREWORD

This thesis was done as a part of a MIMEPA research project at the University of Oulu. I would like to thank Docent Janne Aikio for supervising this thesis and for his guidance and help. Thanks go also to the second examiner Professor Timo Rahkonen. Thanks to Jere Rusanen and other colleagues for providing help when needed. Special thanks to my friend M.Sc. Lauri Peltoniemi for prolific conversations and mental support.

Oulu, March 4, 2021

Sauli Haukka

LIST OF ABBREVIATIONS AND SYMBOLS

AC	alternating current
ACPR	adjacent channel power ratio
AM-AM	amplitude-dependent amplitude distortion
AM-PM	amplitude-dependent phase distortion
CMOS	complementary metal-oxide-semiconductor
BOX	buried oxide
DAC	digital-to-analog converter
DC	direct current
DPD	digital predistorter
DRC	design rule check
DS	derivative superposition
FBB	forward body bias
FDSOI	fully depleted silicon-on-insulator
FU	fundamental tone
HB	harmonic balance
IC	integrated circuit
IM	intermodulation
IM_3	3^{rd}-order intermodulation distortion
IM_3L	lower 3^{rd}-order intermodulation distortion at $(2f_1-f_2)$
IM_3H	higher 3^{rd}-order intermodulation distortion at $(2f_2-f_1)$
IM_5	5^{th}-order intermodulation distortion
IMD	intermodulation distortion
LVS	layout versus schematic
MIMO	multiple-input and multiple-output
MOSFET	metal-oxide-semiconductor field-effect transistor
NFET	n-channel field-effect transistor
NMOS	n-channel metal-oxide-semiconductor
PA	power amplifier
PAPR	peak to average power ratio
PDSOI	partially depleted silicon-on-insulator
PEX	parasitic extraction
PFET	p-channel field-effect transistor
PMOS	p-channel metal-oxide-semiconductor
SLVT	super low voltage threshold
SOI	silicon-on-insulator
TRX	transceiver

a_n	n^{th}-order nonlinearity coefficient of the Taylor series
A	amplitude
C	capacitance
f	frequency
f_0	centre frequency
f_1	lower fundamental frequency
f_2	higher fundamental frequency
g_n	small-signal n^{th}-order transconductance coefficient
g_{na}	small-signal n^{th}-order transconductance coefficient of auxiliary device

g_{nm}	small-signal n^{th}-order transconductance coefficient of the main device
g_{nn}	small-signal n^{th}-order transconductance coefficient of NFET
g_{np}	small-signal n^{th}-order transconductance coefficient of PFET
i_d	small-signal drain current
i_{da}	small-signal drain current of auxiliary device
i_{dm}	small-signal drain current of the main device
i_{dn}	small-signal drain current of NMOS
i_{dp}	small-signal drain current of PMOS
i_{out}	small-signal output current
IP1dB	input 1 dB compression point
L	inductance
mmWave	millimetre wave
P1dB	1 dB compression point
P_{IN}	input power
P_{OUT}	output power
V_{DD}	positive supply voltage
v_{gs}	small-signal gate-to-source voltage
V_{SS}	negative supply voltage
Δf	tone spacing f_2-f_1

1 INTRODUCTION

In modern telecommunications systems linearizing the wanted signal is a crucial part of analog and digital circuit design. When a signal is handled with active electronics, there will be nonlinearity present that distorts the signal. With linearization, the distortion is aimed to be cancelled and thus the performance of the whole system gets better.[1]

Commonly, the digital predistorter (DPD) is used to linearize the signal. In [2] and [3] DPD is stated to be the most used technique nowadays. Traditionally, digital predistorter is an efficient way to produce the required linearity to one big and powerful solid-state power amplifier (PA). But due to the telecommunication standards evolution, this is getting more complicated. With standard such as 3GPP FR2, the increase in data rate is aimed to be achieved by increasing the bandwidth. The wanted bandwidth is available at mmWave (millimetre wave) frequencies up to 50 GHz [4]. Furthermore, with mmWaves, the MIMO (Multiple-Input and Multiple-Output) transceivers (TRX) with beamforming are used. MIMO transceivers might have even thousands of antennas, and thus the power needs to be divided between all the antennas, preferably with a beamforming capability [5]. Even with the best power amplifiers and by using the high frequencies, one big PA is not the optimal solution for these types of transceivers. A common solution for such transceivers is to use small integrated circuits (IC) to cover one antenna or one antenna group. The single IC would consist preferably of a complete TRX and a power amplifier with an additional simple analog predistorter. The predistorter is aimed to provide improvement to the linearity in the first place, which then could be enhanced with DPD later on.

This thesis consists of the following. Chapter 2 presents the theory behind the nonlinearities in active circuits. The second part of this thesis, Chapter 3, goes through the design and theory of the proposed circuits. In Chapter 4 the basics behind the layout and measurement implementation are presented. Also, the main layout verifications concepts are introduced. The simulation results of the circuits are presented in Chapter 5. In Chapter 6 the designed circuits are added in front of a power amplifier. The simulations show the effect of the predistorter circuits prior to the power amplifier and verify them in a more practical environment. Chapter 7 provides a discussion and Chapter 8 is a complete summary of the thesis.

2 THEORY

Section 2.1 presents the theory behind nonlinearity and distortion in analog circuits. In section 2.2 linearization is introduced.

2.1 Nonlinearity and nonlinear distortion

Linear system is somewhat self-explanatory. The output of a linear system is linearly proportional to its input. If the system has unity gain, with any amplitude of the input signal the output has the same amplitude. With nonlinear systems, the output signal does not follow the input signal similarly. The gain of the system varies with different input signal amplitude, thus causing the output signal not to be linear when compared to the input signal.

Memoryless nonlinearity in a circuit can be modelled using a power series as

$$y = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + \cdots, \tag{1}$$

where y and x are the output and input signals, respectively and a_0, a_1, a_2, a_3 are coefficients [6]. a_1 in (1) is a linear gain, while a_2 and a_3 represent 2nd and 3rd order memoryless nonlinearities.

In addition to the already mentioned nonlinearity in the gain, nonlinear systems also suffer from spectral regrowth which can be calculated from (1). When a multitone signal is applied to a nonlinear circuit, it produces intermodulation (IM) products and harmonics. These intermodulation products are sums of fundamental carrier frequencies with different combinations. The most interesting of these is the third-order intermodulation (IM_3) products which occur close to the fundamental tones.

The simplest way of presenting these intermodulation products and spectral regrowth is with a two-tone input signal

$$x = A_1 \cos(2\pi f_1 t) + A_2 \cos(2\pi f_2 t) \tag{2}$$

where A_1 and A_2 are the amplitudes of the fundamental tones, and f_1 and f_2 are their frequencies [6]. When a signal with two fundamental tones (2) is driven into a nonlinear circuit modelled with (1), the nonlinearity causes intermodulation products as seen in Figure 1. Harmonics are multiples of individual fundamental tones and intermodulation products are mixing results of both fundamental tones.

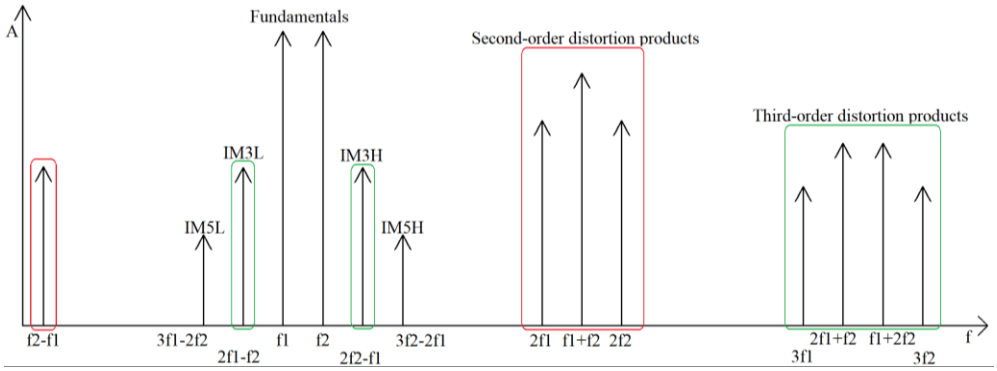

Figure 1. Frequency components caused by nonlinearities.

On sidebands of the fundamental signals, the lower third-order intermodulation product (IM_3L) is at a frequency of $2f_1$-f_2 and the higher third-order intermodulation product (IM_3H) is at frequency of $2f_2$-f1. These IM_3 sideband products are the most interesting due to the fact that they appear close to the fundamental signals. Therefore, the filtering of these signals is not possible as it would be for the harmonics (with an assumption that the harmonics would not overlap caused by too wide bandwidth relative to the centre frequency). As can be seen from Figure 1 the harmonics and IM products around them, marked with red and green, are at much higher frequencies. Because of that, they are easier to filter out. With IM_3, and IM_5 (fifth-order intermodulation), products being close to fundamentals, the IM sideband levels need to be low enough. The higher-order intermodulation products, such as seventh and ninth, also forming sideband products, are not that dominant and thus, are not as interesting.[7]

As it is explained in [6 p. 21-22] and [7] the IM_3 products at sideband are a combination of second harmonics, at frequencies of $2f_2$ or $2f_1$, and second-order distortion at the baseband with frequencies of f_2-f_1 and f_1-f_2. This causes the sidebands IM_3L and IM_3H to be frequency dependant and so, can cause the sidebands to be asymmetric. [6][7][8][9]

2.1.1 AM-AM and AM-PM

A common way of presenting linearity of a circuit is with amplitude modulation as a function of input amplitude (AM-AM), which is also known as amplitude-dependent amplitude distortion. AM-AM describes the input-output linearity of fundamental tones. In addition to AM-AM, a memory that all nonlinear systems experience, causes a phase shift in the fundamental tone [9]. This phase shift can be presented with phase modulation as a function of input amplitude (AM-PM), also known as amplitude-dependent phase distortion. By using the fundamental tone from (1) with four different values of a_3, different cases of AM-AM and AM-PM are illustrated. In Figure 2a) the coefficient a_3 has an equal phase to a_1 causing the fundamental tone to expand whereas in Figure 2b) the a_3 phase is opposite to a_1 (180-degree phase-shifted) causing compression. Figure 2c) illustrates expansion and AM-PM caused by complex a_3 value with a 45-degree phase shift to the tone. Complex a_3 is also used in Figure 2d) with 135-degree phase shift causing gain compression as well as AM-PM. More accurate details about AM-AM and AM-PM is presented in [1][6 p. 22-24] and [10].

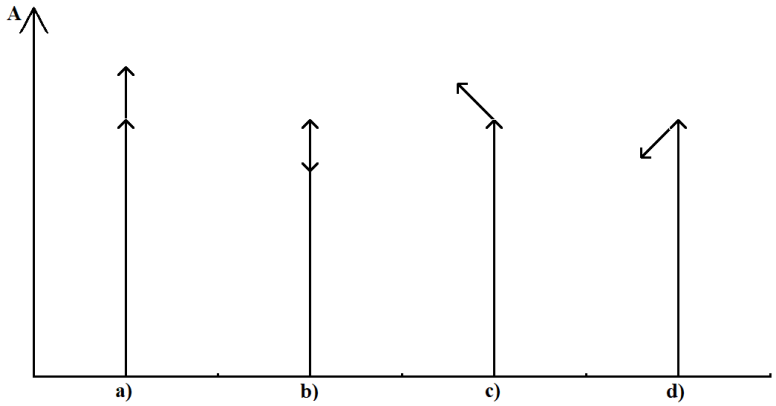

Figure 2. Illustration of AM-AM and AM-PM with different a_3 coefficient values

2.1.2 Saturation

In ideal linear amplification, amplifiers would give linear gain with any power level driven into the input of the amplifier without any compression in gain. Meaning that there is no maximum output power (P_{OUT}) that the circuit can deliver. But in real environment amplifiers have a limited operating range before they reach their maximum output power. Until this point, amplifiers are assumed to produce linear output when compared to an input signal. But as the input amplitude rises, the amplifier reaches its saturation point, where the maximum output power of the amplifier is achieved.

IM_3 also affects the fundamental signal. As the IM_3 level rises 3 dB to each 1 dB of power added to the fundamental signal, the IM_3 contribution to the fundamental signal can be seen at high input amplitude. In (1) the a_3 term sign determines if the IM_3 contribution to the fundamental signal is expanding or compressing the signal. At first, the a_3 value can be a positive contributing as an expansion to the fundamental signal power but as the input amplitude gets higher, the a_3 term changes to be negative. With a negative sign, IM_3 starts to compress the fundamental, causing more and more compression as the input amplitude level gets higher causing the amplifier saturation.

An important figure of merit for saturation is 1 dB compression point (P1dB). This point describes when the gain of the amplifier has decreased by one decibel compared to the linear gain. At this point, the amplifier is usually working with good efficiency, but it is already producing a considerable amount of distortion. After this point, the distortion level is getting higher and gain is, usually, dropping faster and faster until the saturation and maximum output power are reached. Figure 3 presents the output power of an amplifier as a function of input power (P_{IN}) with P1dB marked. [7]

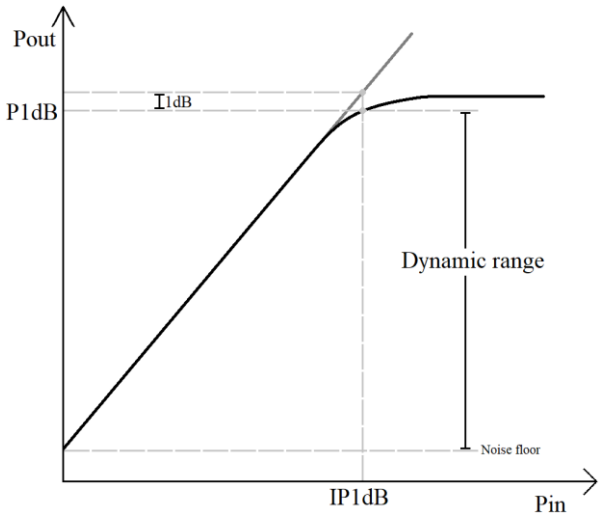

Figure 3. The output power of an amplifier presenting a 1 dB compression point and a dynamic range.

The dynamic range of an amplifier is the range of output level where the amplifier can be used. It is limited by the noise floor at the low end and usually by distortion at the high end. At the high end of the dynamic range, the power amplifier needs to operate far enough from the P1dB to not cause additional distortion or reach saturation. With modern high peak to average power (PAPR) telecommunication signals, it must be ensured that the power amplifier does not exceed the saturation, and therefore some amount of back-off from e.g. P1dB point is needed. If the input signal peaks (could be 6-10 dB higher than the average channel power), with

correctly adjusted back-off the power amplifier still works without reaching saturation. For solid-state power amplifiers, an estimation for back-off is around 10 dB from the P1dB point. By pushing P1dB higher, the power amplifiers back-off is higher, improving the efficiency of the amplifier. Efficiency is important in telecommunications to achieve the best possible linear output power with the lowest possible power dissipation. In [7] is presented a more detailed calculation for the input back-off. [11]

2.2 Linearization

The main goal of linearization is to compensate for the most dominant nonlinearities, which are mainly coming from the PA. Predistortion, feedforward, and feedback linearizations are useful ways to provide linearity to a circuit. Linearization techniques in this section are presented from the analog perspective. [12]

2.2.1 Feed-forward and feedback linearization

In feed-forward linearizers, Figure 4a), the output signal of PA is compared to the input signal, from where the distortion created by the PA can be extracted. This distortion caused by the PA can then be amplified by an auxiliary device and subtracted from the original PA output signal cancelling distortion, leaving ideally only the linear part of the amplified signal to the output of the linearizer. This lowers the level of distortion, ideally to zero. The feed-forward linearizer is a somewhat complex structure needing phase shifters and couplers, which are then causing losses. Due to these losses, a complete cancellation of intermodulation distortion is not achievable. Furthermore, if a power amplifier is working near saturation, feedforward linearizers are not viable solutions. To not cause distortion of its own, the auxiliary transistor needs to work in a linear region. Thus the cancellation cannot be achieved near saturation but it is achievable about 6 dB away from the saturation [13]. [7][12]

On the other hand, feedback linearizers (see Figure 4b) use the output of the amplifier to modify the input of the amplifier to cancel the distortion. This results in an even more complex structure possibly having low pass filters, mixers and local oscillators, to handle gain and phase adjusting [12]. Feedback linearizers tend to suffer from bandwidth limitations due to stability constraints [13]. [7][12]

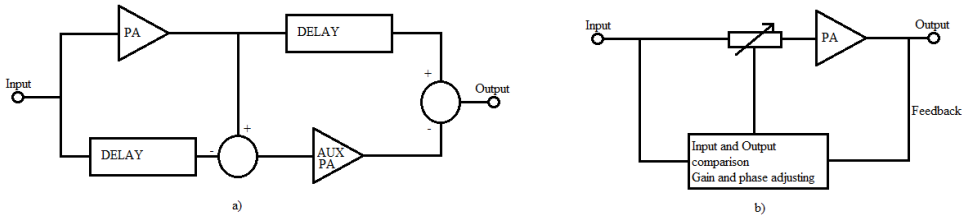

Figure 4. Feed-forward and feedback structures.

2.2.2 Predistortion linearization

Predistortion is a commonly known linearization technique used to cancel the distortion by predistorting the input signal which cancels the distortion generated by the PA. Nonlinear characteristics of the predistorter are the opposite to the main power amplifiers nonlinearities so that the cancellation can take place. Opposite nonlinearities generated in the predistorter can

be such as using IMD for cancellation or compensating the gain compression with expansion. Predistortion linearizers are good solutions if simple, small, and low power application is desired [14]. Predistorter linearizers can provide bandwidth of multiple gigahertz, thus being a good solution for the ever so widening bandwidth [15].

When predistorters are designed to cancel the IM_3 the main thing is that the IM_3 of the predistorter is equal amplitude as the power amplifiers distortion, but at the opposite direction (i.e.180 degrees phase shifted). When two components are in opposite phase, they cancel each other as presented in Figure 5. This is possible for the distortion as it is a deterministic signal. The figure presents a case, where the predistorters cancellation signal is not completely antiphase and the same amplitude. This way the effect of the contributions can be seen more clearly. [6 p. 26-27][7]

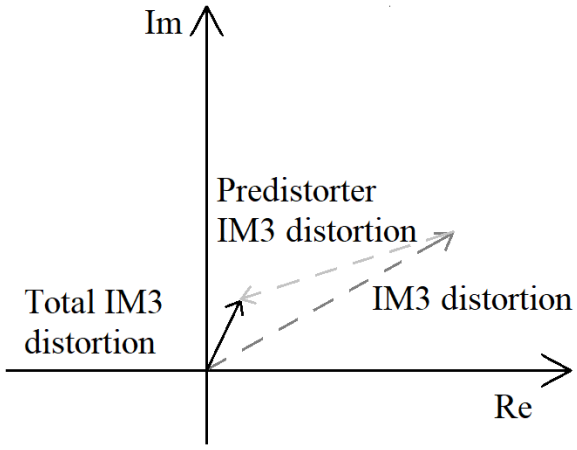

Figure 5. Picture of total IM_3 distortion with predistorter cancellation.

With modulated signals used in telecommunications, spectral regrowth can cause issues. Modulated signal has a carrier wave (fundamental) at a certain band (main channel) containing the information and the adjacent channel caused by the distortion from intermodulation. By cancellation, the adjacent channel power ratio (ACPR) presented in Figure 6 gets better. ACPR represents the ratio of the power of the fundamental signal and the power of the IM sidebands (the adjacent channel). If the power of adjacent channels gets too high, it might interfere with other users at neighbouring bands. [9][13]

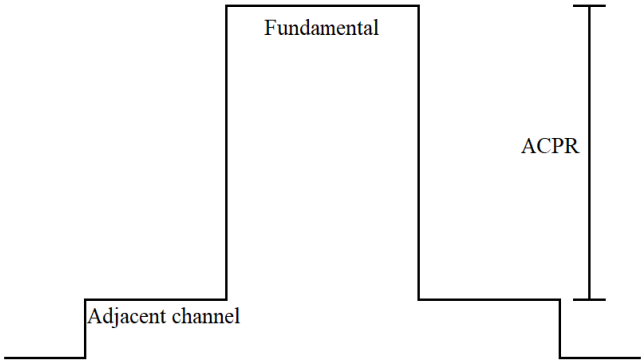

Figure 6. The adjacent channel power ratio ACPR.

What comes to gain compression, it can be improved with expanding predistorter. Expansive predistorter should be designed the way, that it pushes the 1 dB compression point of the amplifier closer to its saturation point, thus providing the amplifiers back-off to be at a higher

power level. In an ideal case, presented in Figure 7a), the gain of the predistorter increases to infinity over the function of input power, and would that way compensate the compression of the main power amplifier at Figure 7b) to form the combined output to be perfectly linear at Figure 7c). This ideal case would also need the amplifier to be able to output more power than it does in the saturation, to achieve the infinite linear output without the output signal clipping. [12]

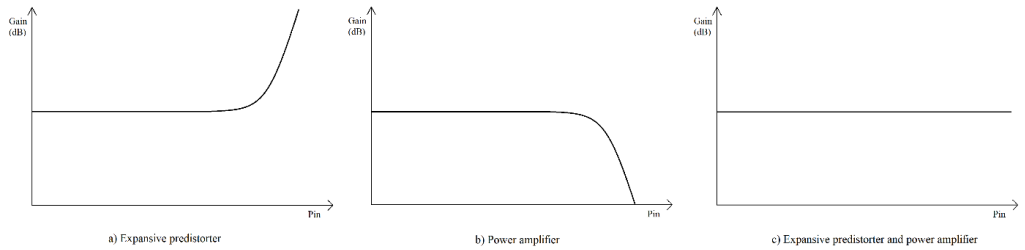

Figure 7. Gains of a) expansive predistorter, b) power amplifier and c) both combined.

Unfortunately, the ideal is not practise. What can be done is somewhat expansive characteristics having predistorter which then, added to an amplifier, linearizes the operation at higher power levels (improvement is wanted around 1dB compression point) [16]. Linear operation at higher power levels is desired because the power amplifiers have higher efficiency near saturation. [7]

3 CIRCUIT DESIGN

The main intention of this thesis was to design a simple predistorter circuit using 22nm CMOS (Complementary Metal-Oxide-Semiconductor) FDSOI (fully depleted silicon-on-insulator) technology. Two circuits were designed to produce different solutions for linearization by using derivative superposition (DS) circuits as a base.

Section 3.1 presents the theory behind the derivative superposition method, which is followed by the designs chosen for this thesis in sections 3.2 and 3.3.

3.1 Derivative superposition

Derivative superposition is commonly known linear-circuit topology [17][18][19]. It is referred to be "a special case of the feedforward technique" [19]. The operation of the topology can be explained via transistors output AC (Alternating Current) drain current which can be presented in a form of polynomial expansion, presenting the nonlinearity similarly as in (1)

$$i_d(v_{gs}) = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + \cdots \quad (3)$$

As mentioned, (3) presents NMOS (n-channel Metal-Oxide-Semiconductor) transistors small-signal drain current, from where it can be seen that the drain current is controlled by the gate to source voltage. V_{gs} is multiplied by small-signal transconductance coefficients, (g_1, g_2, etc.) which are dependent on the operating point of the transistor. The one term, that is the most interesting is the third-order term. At low frequencies, it defines the strength of third-order intermodulation distortion which, as explained earlier, is usually the most dominant source of nonlinearities. Of course, this is not the only factor contributing to the actual IM_3, but certain assumptions can be made to simplify the calculations. [17][18]

The third-order term (and other coefficients) of the Taylor series is dependent on the bias voltage and input signal. In the Taylor series, the g_3 term keeps its value if V_{gs} or input signal level does not change, but by changing the operation point, the g_3 term changes and needs to be recalculated. This behaviour of the coefficients explains the capability of adding up two signal components with opposite values, phase, or sign, to cancel each other by adjusting the bias voltage. Values of g_3 are positive when a transistor is biased in a weak, or moderate, inversion region and the negative values occur when a transistor is biased to a strong inversion region. To be able to use these in practice there must be main and auxiliary transistors or amplifiers, to be used in two different operating regions. [17][18][19]

3.2 Conventional derivative superposition

3.2.1 Theory

The conventional derivative superposition method uses two parallel NMOS transistors. The drain current of each transistor is presented in (3) and as they are summed up in a parallel transistor setup, it causes the following

$$i_{out} = i_{dm} + i_{da} = (g_{1m} + g_{1a})v_{gs} + (g_{2m} + g_{2a})v_{gs}^2 + (g_{3m} + g_{3a})v_{gs}^3 + \cdots \quad (4)$$

where i_{dm} and i_{da} are drain currents of the main transistor and the auxiliary transistor, respectively. From here it can be seen that when g_{2m} and g_{2a} are added, and as they do have the same sign, the second-order intermodulation product gets higher, which is a slight downside of the design. On the other hand, the odd terms g_{3m} and g_{3a} are also summed, but as they are biased to have opposite signs, they cancel each other and thus IM_3 level gets lower. To achieve the maximum amount of improvement for IM_3, the two terms have to be an exact opposite phase and the same amplitude as was illustrated in Figure 5. [18][19]

3.2.2 Design

Even though it was stated that the derivative superposition circuit would be a feedforward linearizer, conventional DS could also be considered as a compromise between feedforward and predistortion linearizers. It has a similar behaviour as feed-forward linearizer which was introduced in Figure 4a) having main amplifier and auxiliary amplifier, but it does not use the output of the main amplifier for the distortion cancellation. This results in the fact that the circuit does not need any delay components and as it is added in the front of PA it also fulfils some of the predistortion linearizer criteria in [7] and [12].

In Figure 8, the schematic of the design is presented. Because both devices, M_1 and M_2 are dimensioned to be equal and input capacitances and resistances are the same, in this circuit, there is no difference between which one is considered as the auxiliary device and which one the main device, as it is determined with the biasing of the transistors.

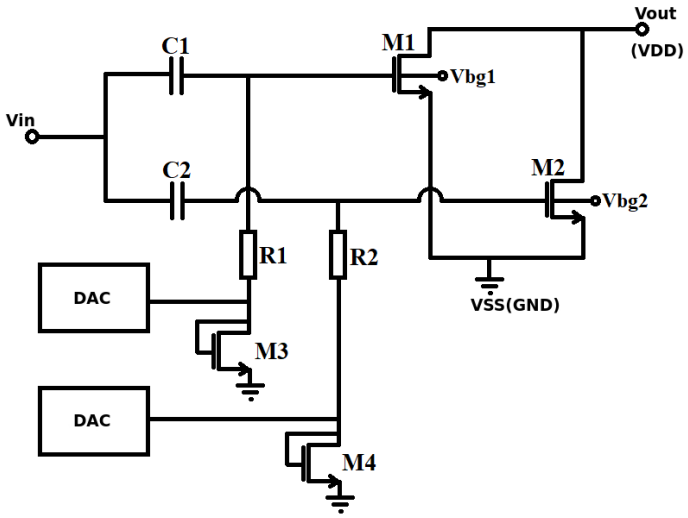

Figure 8. The schematic of the conventional derivative superposition circuit.

Both of the transistors are driven from the same input signal but use separate capacitors at the input side to isolate the different gate biases. The gate biases are created using individual DAC (Digital-to-Analog Converter) for each gate. The supply voltage (V_{DD}) is provided from the common output node. Usually, the V_{DD} would be fed through a choke inductor to prevent the signal to leak to the DC (Direct Current) supply, and the DC capacitor would be used to isolate the output from DC voltage. These parts were left out from the design as DC will be fed via external bias-tee during the measurements.

What is seen in Figure 8, is that also back-gates (V_{bg1}, V_{bg2}) [20] for the transistors M_1 and M_2 are enabled. Back-gates of the transistors provides an alternate way of biasing the transistors

and will be presented further in section 4.1.1. With back-gates enabled, the circuit can be biased in multiple ways providing more possibilities for simulation and measurement purposes.

3.3 Complementary derivative superposition

3.3.1 Theory

As of conventional derivative superposition method is a good way to reduce the unwanted IM_3 it has its downsides. Because the 2nd order terms add up, the design is very sensitive to 2nd order nonlinearity. Complementary derivative superposition, using NMOS as well as PMOS (p-channel Metal-Oxide-Semiconductor) transistors, on the other hand, is capable of cancelling both even and odd-order distortion.

The output current of complementary derivative superposition is calculated as

$$i_{out} = i_{dn} - i_{dp} \tag{5}$$

and when the individual currents are examined, it can be seen why both even and odd-order terms are decreasing when biased correctly. Small-signal drain to source current for PMOS device is as follows

$$i_{dp} = -g_{1p}v_{gs} + g_{2p}v_{gs}^2 - g_{3n}v_{gs}^3 + \cdots \tag{6}$$

From equations (3) and (6) can be seen that the signs of individual terms are different between the devices. When equations (3) and (6) are added to equation (5) the result is

$$i_{out} = (g_{1n} + g_{1p})v_{gs} + (g_{2n} - g_{2p})v_{gs}^2 + (g_{3n}+g_{3p})v_{gs}^3 + \cdots \tag{7}$$

Where g_{1n}, g_{2n}, etc. are NMOS transistors coefficients and g_{1p}, g_{2p}, etc. are PMOS transistors coefficients. At first glance, it might seem that only the second-order terms are cancelling each other, but it happens also with 3rd-order the same way it does in the conventional design. When the transistors are biased correctly the g_2 terms of both transistors have the same sign and at the same time, the g_3 terms have different signs. Hence, both terms are cancelling. However, there is a slight difference between optimal values for 2nd and 3rd-order cancellation. Thus, depending on which is the desired quality, the optimization of gate biasing needs to be done. [19]

3.3.2 Design

Although for a complementary circuit there is room for adjustment between second and third-order, neither of them were priorities when the circuit, in Figure 9, was designed. The conventional DS circuit was designed first to provide improvement and linearization in the perspective of lowering the IM_3 level at sidebands. The other sides of linearization were desired to be covered too, so an expansive circuit was needed. The first assumption was, that by resizing the transistors at the conventional design, some expansion could be achieved. After some testing was done, expansion was not achieved as wanted. By using the complementary derivative superposition structure instead, it was possible to achieve expanding behaviour for the circuit and keeping it simple. The base of the circuit was the complementary derivative superposition, and as stated before, it can be considered as a feed-forward linearizer. In this case, the properties

of the circuit were modified, so that the cancellation is not happening similarly for the IM_3 as in conventional DS. By providing expansive gain, the circuit can be considered more as a predistortion linearizer.

In Figure 9 the transistor M_1 is a PMOS transistor, which is acting as an auxiliary device and the main device M_2 is an NMOS transistor. Input is driven, as in the other design, to both transistors and gates are biased by using DACs. The difference for this circuit is that the choke inductor L_1 was added, as well as a DC capacitor C_3, both on the PMOS transistors source. A choke inductor is needed, to isolate the signal leaking to the V_{DD}. This affected the performance by not grounding the PMOS device in the small-signal model and could be fixed with a bypass capacitor to the ground. This allows the PMOS transistors source to be grounded from an AC perspective, but the supply voltage is still delivered to the circuit.

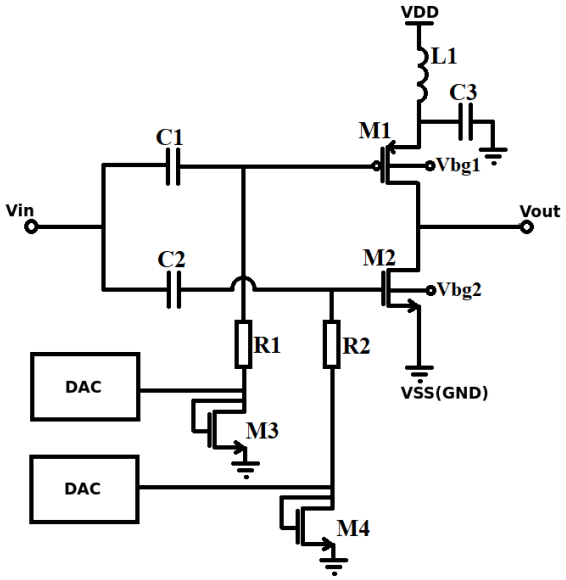

Figure 9. Schematic of the designed complementary derivative superposition circuit.

From the small-signal point of view, this causes the design to have LC parallel circuit at the source and, consequently, the resonance frequency may cause some issues at the circuit, if not dimensioned properly. That issue will be covered in Chapter 5.

This complementary structure is a variation of a push-pull type amplifier and the expansive behaviour comes from the circuit biasing itself when more power is added to it. When more power is driven into the input of the amplifier, the voltage at the transistors shared drain, which is also used as the output node, rises. This causes the main transistor to conduct more which is seen by the gain expansion.

For this structure, to have the optimal IM_3 improvement these two transistors should be equal-sized. Furthermore, the bias points need some tuning. Especially the bias of the auxiliary transistor needs adjusting so that the transistor operating point is biased more to the weak inversion.

4 LAYOUT DESIGN

Chapter 4 presents the layout design part of the proposed circuits. Section 4.1 presents the micromanufacturing technology used followed by Section 4.2 presenting the implemented layout with a background. From section 4.3 to 4.5 some concepts of layout design, in general, are covered.

4.1 CMOS FDSOI

The micromanufacturing technology used in this project is CMOS fully depleted silicon-on-insulator (FDSOI). This technology allows low leakages, power savings, better noise figures and switch performance and much more when compared to bulk MOSFET (Metal-Oxide-Semiconductor field-effect transistor) devices. [21]

Silicon-on-insulator (SOI) technology is based on a thin oxide layer buried inside the transistor, referred to as BOX (Buried Oxide). This oxide layer takes apart the top layers (drain, gate, source, etc) of the device from the base silicon substrate, whereas the bulk MOSFET transistor is connected straight to a bulk silicon wafer. This thin layer of oxide plays a big part in lowering the leakages in the transistors. As can be seen from Figure 10, SOI technology leaves a smaller gap from where the current, shown as yellow arrows, can flow through, whereas in bulk MOSFET the current has much more room to leak elsewhere in the, much thicker, substrate. Due to the BOX in SOI, the junction capacitances are reduced with a large variety of other benefits. [21]

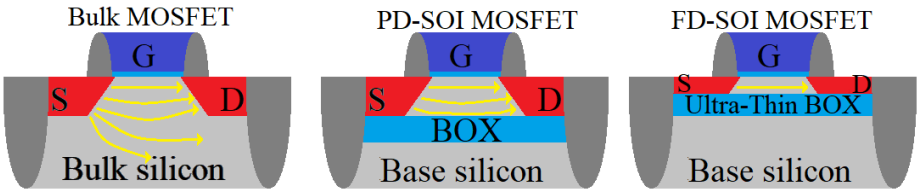

Figure 10. Cross-sections of bulk MOSFET, PDSOI MOSFET and FDSOI MOSFET.

The difference in the body is mainly what separates the partially depleted (PDSOI) device from the fully depleted. What determines if the SOI is fully or partially depleted is the thickness of the silicon. The Transistor channel has a depletion depth, which is the depth of the channel from where the current can flow through the silicon. When the depth of the depletion is greater than the thickness of the silicon, the transistor is fully depleted. On the partially depleted structure, the oxide layer and the body are considerably thicker than in FDSOI. This thickness of the upper silicon is crucial for the floating body effect. In PDSOI the floating body effect can have a significant effect on the operation of the transistor, whereas in FDSOI the effect is minimized with the thinner body. [21]

These changes between partially and fully depleted technologies create some different features between similar technologies, benefitting the FDSOI. The FDSOI is more immune to the kink effect, for example. [21][22]

4.1.1 Body biasing

Body biasing allows an adjustable dynamical range for the transistor threshold voltage. Body biasing is illustrated in Figure 11. Because of the ultra-thin BOX inside the transistor, a voltage

applied to base silicon acts as a back-gate. This lowers the threshold voltage of the transistor by allowing the transistors current flow with a lower biasing of the actual gate.

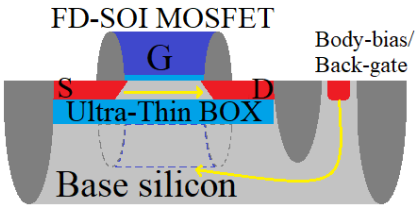

Figure 11. The cross-section of FDSOI with body biasing.

The back-gate biasing opens possibilities to adjust the operation of the transistor to the wanted application on a wide range. According to GlobalFoundries, with back-gate biasing the transistor can be adjusted from a low-power device with less leakage current to the highest performance, operating at high speeds. [20][23][24][25]

4.1.2 Super low voltage threshold

The transistor types that are used in this thesis are super low voltage threshold (SLVT) devices. This means that their normal threshold voltage, even without body biasing is very low. In Figure 12 is presented the used SLVT FDSOI NFET (n-channel field-effect transistor) transistor with 800 mV supply voltage and three different biasing cases. By grounding the gate, the threshold voltage is around 252.8 mV as is presented in Figure 12a). With 600 mV gate bias, in Figure 12b), the threshold voltage is around 257.8 mV.

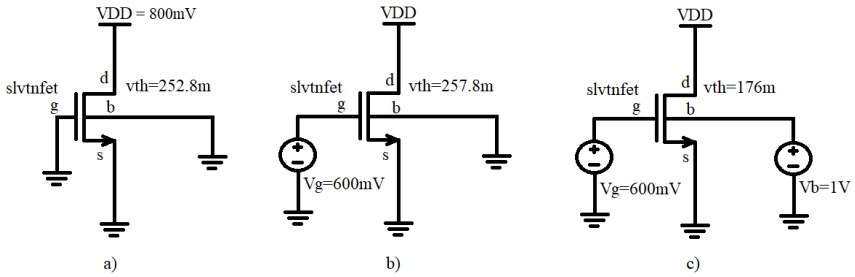

Figure 12. Measured operating points for three threshold voltage cases of SLVT NFETs.

The back-gate body biasing for NFET operates from -0.7 V upwards. Due to the substrate under the transistor, with lower voltages than -0.7 V, the current starts to leak through the substrate to the ground. With forward body biasing (FBB) the threshold voltage can be lowered approximately 75 mV to every 1 V added. This is presented in Figure 12c). At least, in theory, the voltage threshold could be lowered to 0 V by adding around 3.3 V of back-gate bias. This would mean that the transistor is conducting without any gate bias.

4.2 Layout design of the proposed circuits

The designs were implemented by using 22nm CMOS FDSOI technology suited for low power and small-sized IC designs [23]. The first task in the layout design was to place components on the layout and route connections by using different metal layers. The design is meant to be measured using probing and thus the probing pads were added to the layouts.

At first, both circuits were designed to have individual probing pads. These designs would have three pads on each side in order of ground-signal-ground (GSG) probing, meaning that there are two ground pads and the signal pad in the middle. These probing pads would be on each side of the circuit to provide pads for input and output signals. After both designs were made, it was decided that the circuits would be combined to save space on the top layout. The circuits were combined by using GSGSG sets with five probing pads each. The five-pad set, seen in Figure 13, has three ground (V_{SS}) pads and two signal pads between them. This allows both of the designs to have individual pads for input and output signals and combined ground pads, which are all connected. After the combination, the circuits still work as individuals, but a space of over one probing pad in height was reduced. The other inputs, such as DAC controls, supply voltages and back-gate biases are routed on the higher-level layout.

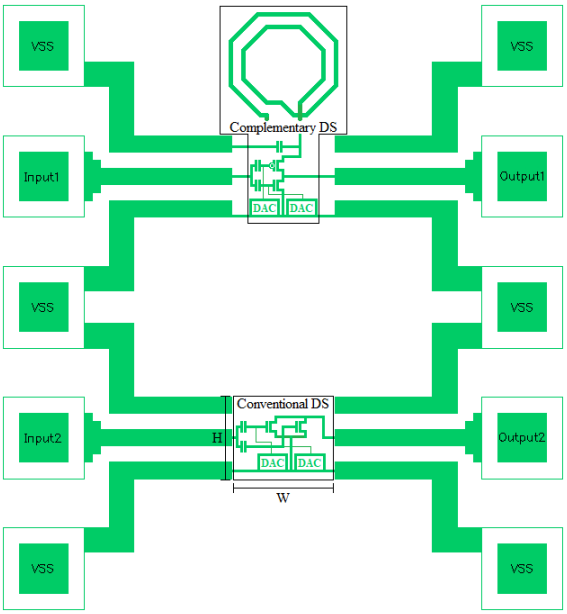

Figure 13. Illustration of the layout of the designed circuit.

Additional reduction of the size of the combined design was achieved when the inductor of the complementary DS circuit was rerouted. The complementary circuit needs an inductor to block the DC supply from the output node. When the inductor was routed to the upper side of the design as is seen in Figure 13, the width of the design was reduced from 54 µm (width of the inductor) to 13.4 µm. Complete dimensions of the design without and with the inductor, are 13.4 µm in width (W) and 34.4 µm in height (H) and 54 µm in width and 118.4 µm in height, respectively.

Because the conventional DS circuit has the output and the transistor drains at the same node, the same pad (output2) can be used to provide supply voltage and to measure the output signal. This is done with the off-chip bias-tee separating the line for the choke inductor and DC block capacitor. By adding the external components to the measurement setup, their effect on the measurement results can be neglected by on-chip calibration, and therefore the more accurate performance of the circuit can be seen. The conventional DS design somewhat determines the width of the whole design by being the wider circuit out of these two. Thus, limiting the gap between the probing pad sets to be at least the width of the design. The conventional design has a width of 22.9 µm and a height of 17.1 µm. The dimension of the whole combined design is 277.6 µm in width and 450 µm in height.

4.3 Design rule check

When designing a layout, design rules are playing a crucial role. Design rules are set for the technology used by the semiconductor manufacturer. Manufacturers need designs to meet certain specifications so that the designs can be manufactured without the risk of chip failure. Design rule checking (DRC) checks the design if these specifications are met and if not, it shows where and what the violations are. According to Synopsys [26], some basic DRC rules are:

- Minimum width
- Minimum spacing
- Minimum area
- Wide metal jog
- Misaligned via wire
- Special notch spacing
- End of line spacing

The chip area used for the design is affected by these rules. The area is determined mainly by the component size and the chosen metal thicknesses and spacings. Hence, components need to be placed so that there is enough room for wiring. [27]

More accurate detail of how DRC operates can be found, for example, from Mentor graphics Calibre Verification User's Manual [28].

4.4 Layout versus schematic

Layout versus schematic (LVS) physical verification is used to check if the designed layout corresponds with the design schematic. LVS uses extracted netlist of the layout to compare it with the netlist of the schematic. When the netlists are compared, the result shows the errors and locations where they occur. Synopsys lists LVS errors into two main categories, extraction errors and compare errors [29].

Extraction errors include:

- Text short and open
- Device extraction error
- Missing device terminal
- Extra device terminal
- Unused text
- Duplicate structure placement

Compare errors include:

- Unmatched nets in the layout/schematic
- Unmatched devices in the layout/schematic
- Property errors
- Port swap errors

As can be seen from the basic sets of errors, LVS checks the wirings, component placing and component properties (including physical sizes). LVS check tries to match layout nets even if they differ from the nets of the schematic to provide more information about the errors. Calibre LVS provides information from two different point of views. It describes the discrepancy in the way if the source circuit is correct or if the layout circuit is correct. Calibre LVS also divides elements, such as nets, instances and ports in comparison result in three different categories. Correct elements are correctly implemented in both source and layout, incorrect elements are certainly wrong and have no matching element in the other circuit. Lastly, unmatched elements cannot be matched with any specific element in the other circuit, or cannot certainly be specified as incorrect [28]. [30]

LVS needs to be error-free so that the parasitic extraction (PEX) can be performed.

4.5 Parasitic extraction

Extracting parasitics from the design is important to achieve the most accurate estimation of the circuits analog operation. Parasitic extraction creates a model of the circuit with parasitic resistances and capacitances (inductances are not extracted for these circuits). The parasitic effects are calculated for devices and wiring in the design and the results are for example used in timing analysis, power analysis, circuit simulation and signal integrity analysis. All the simulation results to be presented are done with parasitic extraction results included unless otherwise stated. [31][32]

5 SIMULATION RESULTS

To design and fully ensure the operation of the circuits, a wide variety of simulations were needed. The simulations and results are presented in this chapter. Even though simulations for both circuits follow the same path, the results are presented separately.

Section 5.1 presents the conventional derivative superposition (DS) circuit testbench, the simulation results and the theory about the simulations. Section 5.2 shows the simulation results and testbench of the complementary DS circuit. The summary of the simulation results is presented in Section 5.3.

5.1 Conventional derivative superposition

5.1.1 Testbench

The testbench for the conventional DS is presented in Figure 14. The testbench consists of ideal grounds, input and output ports, ideal voltage sources covering V_{DD} and back-gate biasing and an ideal choke inductor and capacitor at the output.

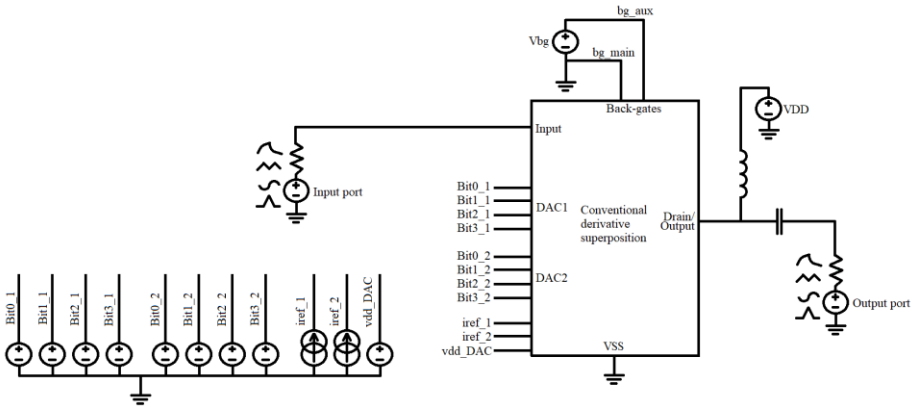

Figure 14. Testbench setup of the design.

To ensure the operation of the circuit, the DC operation points were selected. The V_{DD} of 800 mV is used and V_{SS} (negative supply voltage) equals ground. Those were mainly determined by the drain-to-source voltages (maximum of 900mV) of the transistor and the voltages used in the top layout.

The main idea of the conventional DS operation is presented in Section 3.2 and in [18]. With the values provided in [18], the rough estimate of the gate biases was done. Further biasing of the gates needed more adjustment, which was more accurately done with the usage of HB (Harmonic Balance) analysis shown in Section 5.1.4 to achieve the IM_3 cancellation. The main and auxiliary transistor gate biases were set to 650 mV and 150 mV, respectively.

An ideal bias-tee in a form of a choke inductor and DC capacitor was added to the testbench. This allows the simulations to be done, without the inductor and capacitor affecting the operation of the circuit.

The input port, as well as the output port, was set to 50 Ω load, which attenuates the signal strength and thus simulates the real environment where 50 Ω load is used.

After the schematic and the testbench was implemented, the supply voltage was set and with rough estimates of the gate-biases, the transistor sizing was done. The transistors were sized to

keep the current of the circuit at a reasonably low level, with a target at around 5 mA. At that bias current, the circuit is able to drive enough power to 50 Ω load so that the measurements can be performed reliably. With 800 mV of supply voltage, the targeted 5 mA current was achieved with transistors having W/L (width to length ratio) of 444.9. With this ratio, the actual current achieved was around 4.64 mA.

In the testbench, the back-gates are mainly connected as shown in Figure 14, the main transistor is grounded, and the auxiliary transistor is connected to the voltage source. At the actual design, both are connected to voltage sources separately to be able to be used with adjustable voltages, as it affects the transistor operation if a back-gate voltage is used or not.

5.1.2 Current DAC

Considering the actual measurements of the design, the gate biases were made digitally controllable. This was achieved by using digital-to-analog converters designed specifically for the transistor technique used. These DACs use four-bit control each, leading the DACs to have 16 different output voltages, starting from the DACs to be shut down and providing almost (leakage) zero voltage output. The range of the voltage is scaled by using an external diode-connected transistor, which was implemented in the design with the DAC. The DA converters produce different levels of current, which is then converted to wanted voltage with these diode-connected transistors. All of the DACs use the same 800 mV V_{DD} supply voltage (vdd_DAC in Figure 14) as designed predistorter circuits and 50 µA of a reference current. Further information about these DACs is presented in [33]. In the testbench, the DA converters are controlled with one variable and few lines of control logic code. The control logic code enables each of the four voltage sources seen in Figure 14 (bit0, bit1, bit2 and bit3), depending on which bit is on and which is off. Figure 15 illustrates the DAC output voltages for both transistors corresponding to the bit word. V_{g1} and V_{g2} represent gate biases of the main and auxiliary device, respectively. Being able to control the gate biases of transistors is essential for measuring the operation of the circuits. As will be presented in the simulations further in this thesis, the characteristics of the circuits can be modified with these biases.

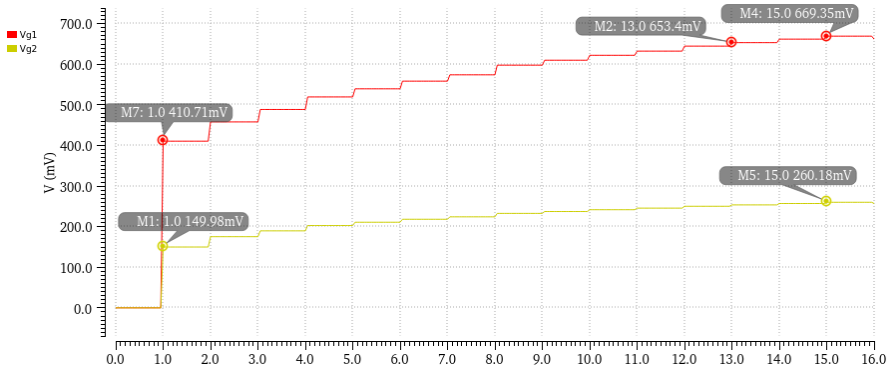

Figure 15. The DAC output voltages corresponding to the used bit word. The red and yellow curves illustrate the gate biases of the main and auxiliary device, respectively.

5.1.3 S-parameters

Scattering parameters (S-parameters) are one way of presenting the properties of the circuit. Here, measured as a two-port network, the S-parameters describes the signal at each port as a

forward and reverse wave at the same point at the same time. S_{11} referred to as the input reflection coefficient, describes how much of the input signal driven into port 1 (input port) reflects back, while the S_{22} is the output reflection coefficient, describing how much of the signal driven into port 2 (output port) is reflecting back. S_{21} presents forward transmission and the same way as the previous ones, it describes the signal at port 2 caused by the signal in port 1, and S_{12} describing the signals at ports vice versa. The most interesting of these four are the S_{11}, S_{22} and S_{21}. [34][35]

An additional parameter of interest is a stability factor (K_f). Rollet's stability factor, as defined in [36], provides information if the circuit is conditionally or unconditionally stable. If the $K_f > 1$, the two-port network is unconditionally stable and remains stable with any given termination. When the K_f is between 1 and -1, the circuit is conditionally stable. Conditionally stable circuits may experience unwanted effects if the termination is not done properly.

In Figure 16 can be seen S_{11}, S_{21} and S_{22} S-parameters of the simulated circuit with marked values for each curve at the operating frequency of 28 GHz. The S_{11} presenting the input ports reflection coefficient shows a value of -0.8 dB and S_{22} has a value of -1.5 dB. Desired value for S_{22} and S_{11} is under 0 dB. The forward voltage gain, S_{21}, presents a value of 0.65 dB, presenting some voltage gain at the network. An important part of this simulation is also the behaviour of the curves at varying frequency. Apart from the low frequencies, the curves are fairly flat. This means, that the S-parameters do not see any resonances or other unwanted effects that are frequency dependant.

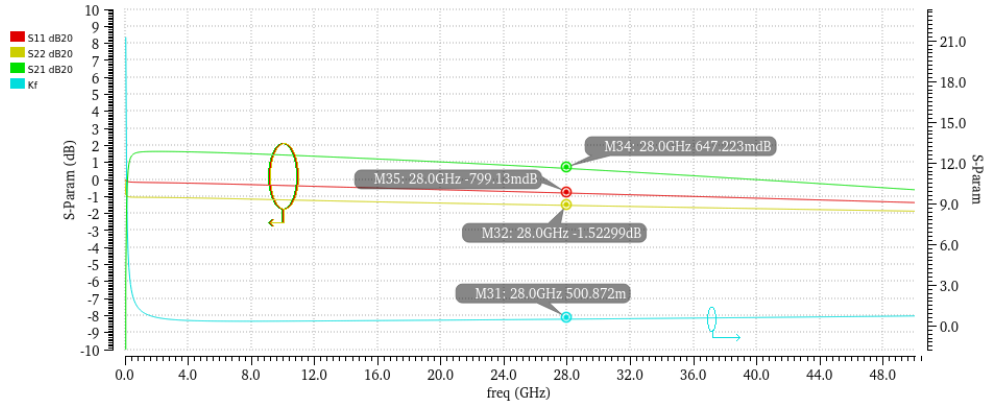

Figure 16. S-param simulation.

The K_f stability factor shows a value of 0.5, meaning that the circuit is only conditionally stable. With 50 Ω input and output loads (set at ports in testbench) the circuit is stable, as both S_{11} and S_{22} are under 0 dB. With different input or output load, this is not the case and some self-oscillation or other kind of instability might occur. To achieve unconditional stability, input and output matching, as well as transistor sizing, might be needed. Matching would be necessary if the circuit would be implemented with another design, where there might be a mismatch between the circuits. Matching was not performed in this thesis. The transistor sizes can also affect the stability of the circuit. With rather small transistors, as used in this circuit, there is a lot of a mismatch causing instability. [34][35]

5.1.4 Harmonic balance simulations

Harmonic balance (HB) is a commonly used nonlinear simulation method. The HB is a large signal analysis that is in this thesis used to simulate the nonlinearity of a circuit as a function of input power, frequency and tone spacing.

5.1.4.1 Input power sweep

By sweeping the input power of the circuit, the nonlinearities such as IM_3 level and AM-AM of the circuit can be plotted. For conventional DS design, these are the simulations presenting the effect of the IM_3 cancellation, providing the results if the theory behind the design is correctly used. The input signal for the simulation is a two-tone signal with a centre frequency at 28 GHz, which is the targeted operation frequency for these circuits. Tone spacing between the two tones is 1 GHz, so the lower fundamental is at 27.5 GHz and IM_3L is thus at 26.5 GHz. The power level of the signals differ a little depending on if the simulated signal is the higher or lower tone, but the characteristics presented in the simulations are still the same. Plotted curves present lower tones of fundamental and intermodulation products unless otherwise is stated.

Simulating the output power gain as a function of the input power, the gain of the circuit can be seen at varying input power levels. As seen in Figure 17 the gain of the circuit is around 8.9 dB with low input power. When sweeping the input to a higher power, it can be seen where the output starts to compress. The P1dB marked as M7 has an output power of -6.5 dBm. At this point, the gain has decreased to 7.9 dB.

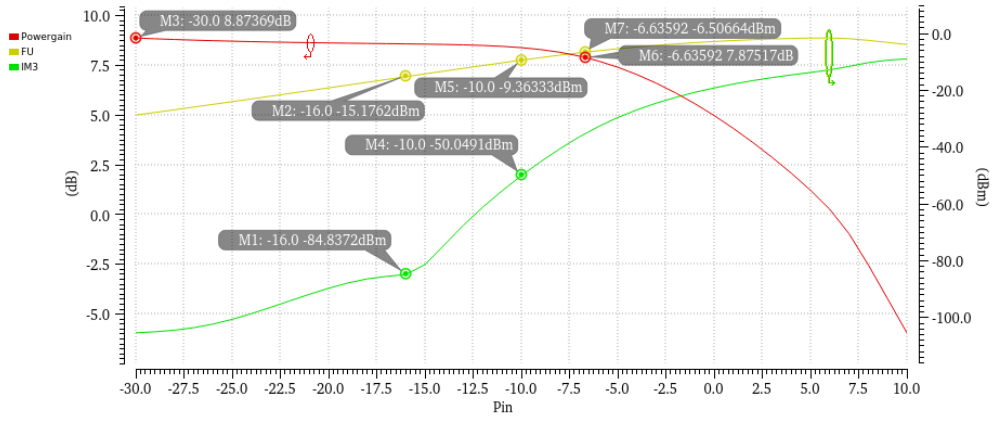

Figure 17. Output power levels of fundamental, IM_3 and power gain as a function of input power in dBm.

In Figure 17 it is also presented lower fundamental and IM_3L output power levels. The fundamental curve presents the AM-AM result, discussed in section 2.1.1, having fairly linear behaviour at small input signal levels, but as the input amplitude rises, the fundamental start to compress.

The IM_3L curve reveals the effect of the IM_3 cancellation behaviour of the circuit. The adjusted sweet spot of the IM_3 is at a P_{IN} of -16 dBm. Thus, with a lower input amplitude than -16 dBm, the circuit is cancelling the distortion and the IM_3 level is not rising at the nominal 3dB/1dB curve. When the input amplitude passes the optimal value, the IM_3 level starts to rise very rapidly. Up until the input amplitude of -16 dBm, the auxiliary transistors IM_3 term has an

opposite sign compared to the main transistor. But as the amplitude rises, at a certain point the phase of the IM_3 term in the auxiliary transistor starts to rotate to be the same as in the main transistor. This causes the IM_3 contribution of the auxiliary transistor to change from cancellation to increasing the total IM_3 level.

Figure 18 shows a comparison of the output IM_3L levels when the auxiliary device is biased correctly versus when the auxiliary device does not have any biasing. The blue and purple curves present fundamental and IM_3L when the auxiliary device is not biased at all. Yellow and green curves present fundamental and IM_3L when the auxiliary device is correctly biased to minimize IM_3.

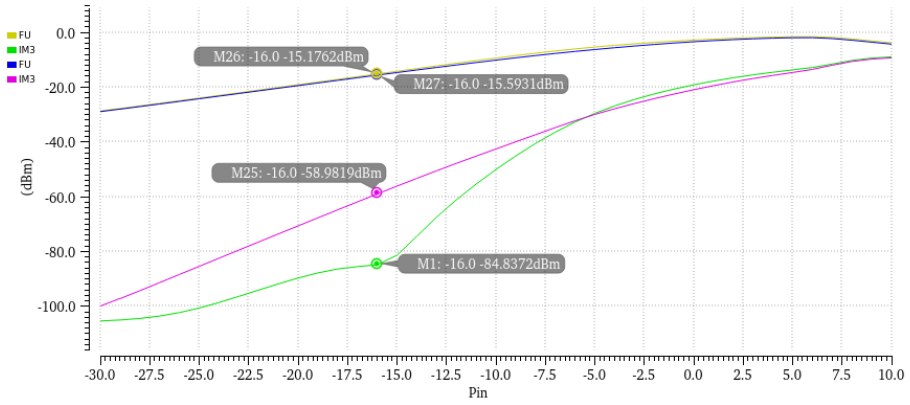

Figure 18. Fundamental and IM_3L output powers of two auxiliary device biasing cases at a function of input power in dBm.

The marker M25 presents a -59.0 dBm IM_3L power level when input power is -16 dBm and the marker M1 with the same input power shows an IM_3L level of -84.8 dBm. The difference in the power levels of the intermodulation products is 25.8 dB. Thus, according to simulations, using the proposed cancellation technique of conventional derivative superposition, a maximum of 25.8 dB improvement in IM_3 is achieved.

Figure 19 presents different cases of biasing the auxiliary transistor. This simulation consists of biasing the transistor using back-gate (BG value), biasing the transistor with normal gate voltage, and a combination of these two.

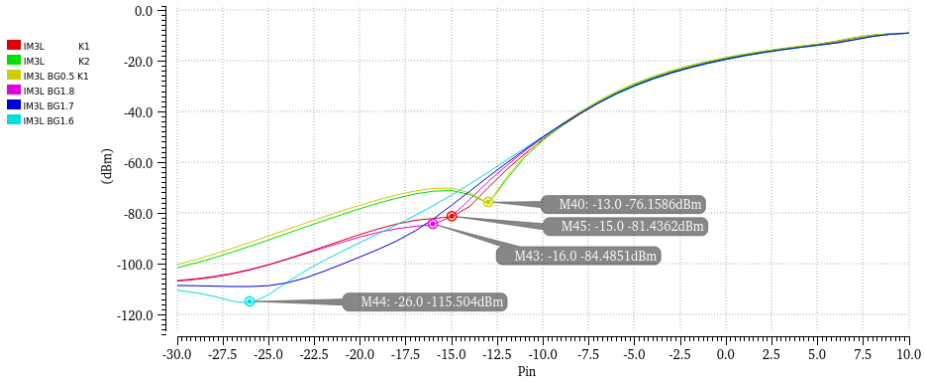

Figure 19. Comparison of different biasing of auxiliary transistor.

By varying the voltage at the back-gate of the transistor, the sweet spot can be adjusted. From 1.6 V to 1.8 V (light blue, blue and violet curves) of back-gate there can be seen a small sweet spot and cancellation at lower amplitudes from the sweet spot. The blue curve shows the

smoothest curve, cancelling the IM_3 well. That implicates that the best biasing for the auxiliary transistor is around 125 mV of gate bias.

With DAC control variable (K) of 1, gate biasing being at around 150 mV, the biasing is fairly similar to when the back-gate is at 1.8 V. Comparing these two curves, red and violet, there is little difference between the sweet spots. However, there is a slight mismatch mathematically, as 1 V of back-gate equals around 75 mV at the gate, so 1.8 V should equal 135 mV. These differences in the operation of the transistors with different biasing are most likely to be seen when the actual circuit is measured. With control variable K = 2 (green curve) the gate bias is around 175 mV. With both biasing methods combined (yellow curve) the back-gate voltage of 0.5 V and the gate voltage of 150 mV added the biasing equals around 188 mV. When comparing yellow and green curves there is, yet again, only a slight difference. With these bias points, the cancellation is not working as intended anymore, causing the IM_3 curve to only have a narrow sweet spot with no cancellation at the lower amplitudes.

5.1.4.2 Frequency sweep

Sweeping the frequency of the input signal instead of input power, the frequency dependency of the circuit can be simulated. This analysis shows if the circuit has any resonances or other similar effects that might occur on certain frequencies. The input signal is a two-tone signal with 1 GHz of tone spacing and an input power of -16 dBm, which is the input power with maximum IM_3 improvement. Figure 20 shows the frequency dependence of the circuit. The gain of the circuit decreases as the frequency gets higher, which is a normal behaviour of an analog circuit. More importantly, there are no clear drops or spikes at any frequency at the simulated frequency range, meaning that in this circuit, there is no unwanted resonances or any other unwanted frequency dependant features.

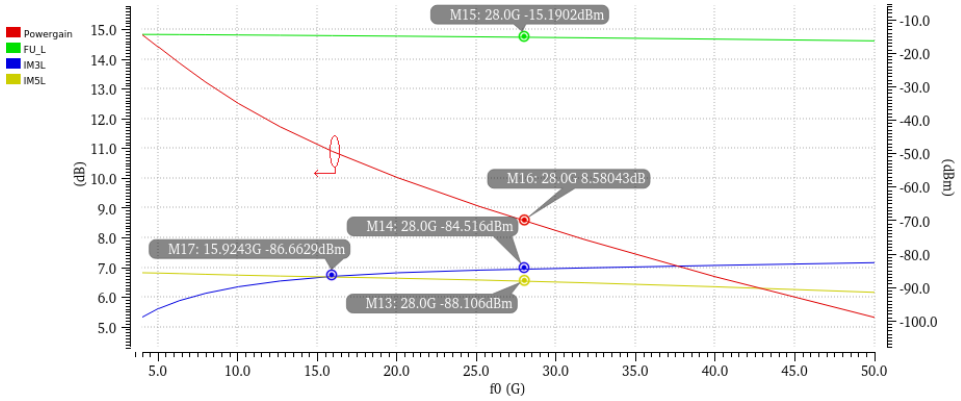

Figure 20. Gain, Fundamental, IM_3 and IM_5 curves as a function of centre frequency in GHz.

The fundamental, IM_3 and IM_5 curves also show somewhat flat behaviour around the centre frequency. Starting from around 20 GHz up to the simulated 50 GHz, there is not that much growth in the distortion level that it would truly affect the signal. The IM_3 curves shape implicates, that the cancellation works even better at low frequencies. What comes to the fundamental, there is a slight decrease in the signal level, but nothing critical.

One point of interest for this circuit, designed to work at around 28 GHz, is the 15.9 GHz frequency. At that point, marked as M17, the IM_3 and IM_5 levels are equal. Furthermore, at even lower frequencies, the IM_3 power level is even lower than the IM_5. Higher frequencies from the marker M17, the levels of both IM products are close to each other. There is still room

for a 5 to 10 dB of improvement for IM_3, but after that point, linearizing the signal even further would also need some form of improvement of the IM_5.

5.1.4.3 Tone spacing

Tone spacing presents the bandwidth of the input signal at simulations. Tone spacing can be presented as

$$\Delta f = f2\text{-}f1 \tag{8}$$

where f_1 and f_2 are the fundamental frequencies and Δf is the tone spacing. As can be seen from Figure 21 the more there is space between the lower and the higher tone, the wider bandwidth of the signal it represents.

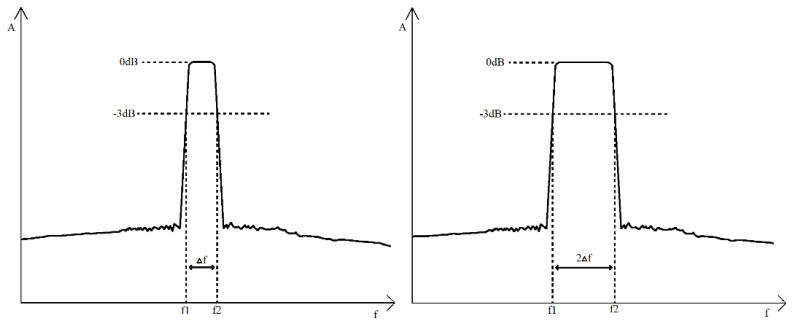

Figure 21. A bandwidth of a signal presented with two different tone spacing values.

By sweeping the signal power as a function of the tone spacing, the effect of wider bandwidth to the signal can be seen. With the tone spacing sweep, wideband performance can be evaluated. Also, by sweeping the tone spacing, some memory effects of the signal can be detected. These effects might worsen the performance of the linearizing circuit. [6 p. 24-25]

Figure 22 presents higher and lower tones of fundamental, IM_3 and IM_5 as a function of tone spacing. The tone spacing is swept from 1 kHz to 2 GHz so that the behaviour can be seen with a wide range of tone spacing for the circuit. The centre frequency of the input signal was 28 GHz and input power was -16 dBm, so the tone spacing simulation is seen at the sweet spot (i.e. maximum point of IM_3 cancellation). The markers are placed to points with the largest difference of the IM_3 tones and to 1 GHz, which is the tone spacing used at other simulations. The simulations present the circuit to be wideband at least up to 2GHz of bandwidth. There are no significant memory effects or nonlinearities in the whole simulated band. There is a small difference in the levels of higher and lower IM_3 products, but as the level of the IM products is so small (below 68 dBc) and the change as a function of tone spacing is 4 dB at maximum, there are no real issues and the circuit is performing well.

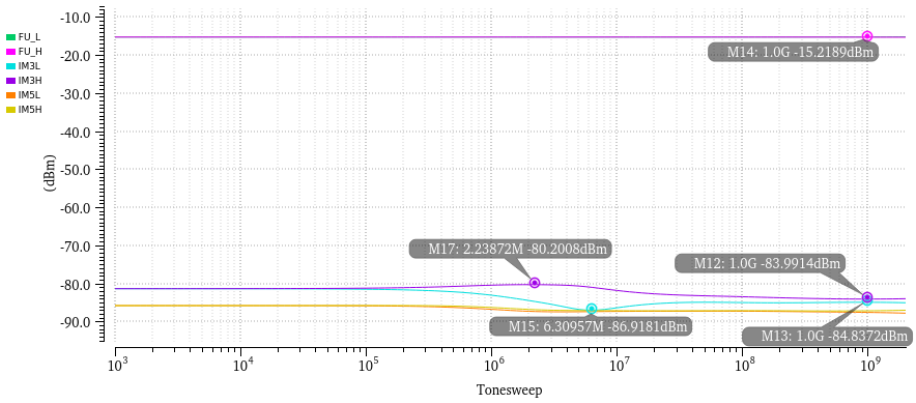

Figure 22. The output powers of fundamental, IM_3 and IM_5 as a function of tone spacing.

5.1.5 Transient analysis

Transient analysis for the circuit was done to observe the stability of the circuit as a function of time. With transient analysis, it is possible to verify, if the circuit starts to self-oscillate with input pulse revealing unwanted instability.

For the transient analysis, the input is a current pulse with a width of 500 fs and with a rise and a fall times of 100 fs. When the pulse is up, the value is 1 mA. The input port is replaced by a setup including a current source generating the wanted current pulse and a parallel 50 Ω resistor. The result of the transient analysis, in Figure 23, presents no instabilities. The output voltage seen in the figure peaks at the start, but immediately after that, the circuits output voltage stabilises. There is a slight variation in the voltage after the first peak, but as its value is between -0.5 µV and 2 µV, the values are just numerical, and not presenting ringing or instability.

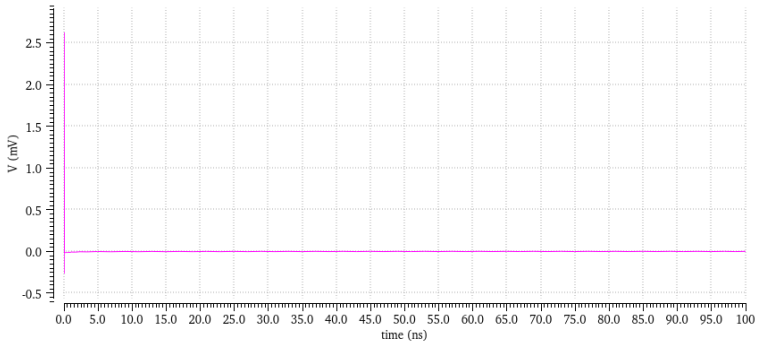

Figure 23. Transient analysis result showing output voltage as a function of time.

5.1.6 The effect of parasitic extraction

Presented in Figure 24, the difference in the values provided has significant change when simulated completely from schematic compared to when simulated with parasitics extracted.

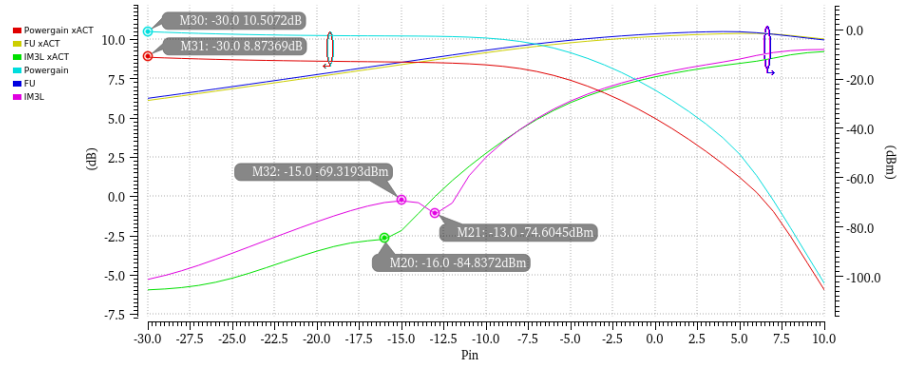

Figure 24. Comparison of the gain, fundamental and IM_3 with and without parasitic extraction.

When the parasitics are extracted, it is clear that the gain of the circuit will be affected. The main shape of the gain curve as a function of input power remains similar, but the power gain itself drops from 10.5 dB to 8.9 dB.

What is notable, is that with IM_3 the curve shapes differ a lot. The curves have a similar shape at high amplitudes, but at the fixed sweet spot and below, the power levels have much of a difference. The circuit with the parasitics included (green curve) seems to cancel the IM_3 better than the circuit without parasitics (purple). Additionally, the sweet spots of the curves are at different input amplitudes.

From the change of place of the sweet spot and according to the results from Figure 19, one possible reason for why the IM_3 level is changing the way it is might be the change in biasing. When the parasitics are considered, all the signal levels differ from the original, so the biasing might even be more optimal with the parasitics included, thus providing better cancellation. To inspect the effect even further, Figure 25 presents an alternative way to compare the difference in the IM_3 levels. When the IM_3 levels are compared as a function of output power, the effect of the gain on the distortion is neglected. The result confirms that the change in the sweet spot place is not due to the difference in the gain.

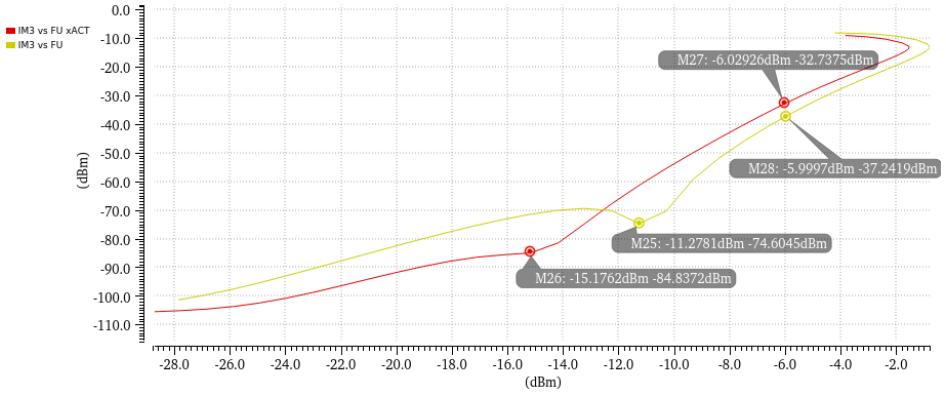

Figure 25. IM_3L output power as a function of fundamental output power with (red) and without (yellow) PEX included.

5.2 Complementary derivative superposition

5.2.1 Testbench

There are very few changes to the testbench for the complementary DS circuit compared to the conventional DS circuit testbench presented earlier. Input and output ports used are the same

as well as DAC controls. The main difference in the testbench shown in Figure 26 is the V_{DD} supply and output port. Because in this circuit, the supply voltage is at a different node than the output, the supply voltage is brought into the circuit from the top layout itself, not from the common output port. The choke inductor is not seen in the testbench because a library component is used as a part of the circuit. Back-gates are enabled to be used for this circuit, but in the testbench, they are mainly connected to the ground. The back-gates are usable and connected to adjustable voltage supplies in the actual design.

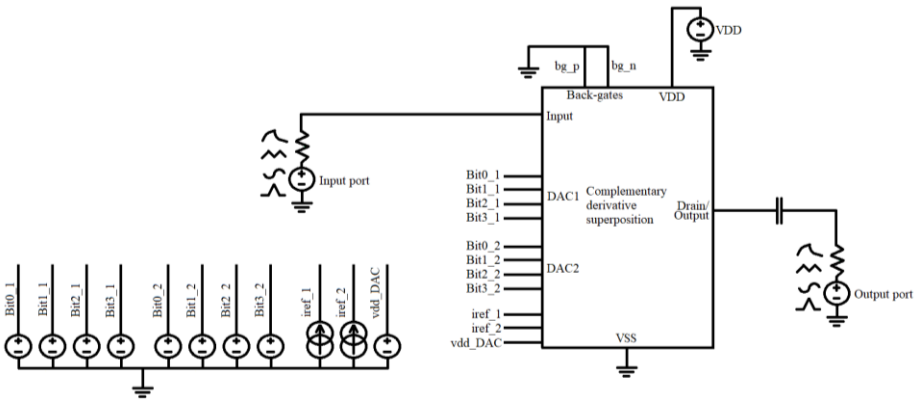

Figure 26. Testbench of the design.

After the testbench was modified from the conventional circuit to fit the complementary design, the transistor sizing was done. By using equal-sized transistors, a similar IM_3 cancellation was achieved than with the conventional design. After changing the length of the upper PMOS transistor, expansion was achieved. Both transistors have the same width, but the W/L ratio between the transistors differ. The NMOS has a W/L ratio of 1111.1 and the PMOS has a ratio of 285.7. This allows the PMOS transistor, controlling the drain current for both devices, to rise more as input power increases, which causes more gain to the circuit.

5.2.2 S-parameters

Figure 27 shows the S-parameters and Rollet's stability factor. From the stability factor, K_f can be seen that the circuit is unconditionally stable. As stated in [36], if the stability factor is greater than 1 the circuit is unconditionally stable and with K_f being 4.5 at a frequency of 28 GHz this condition is achieved. Further inspection of the circuit shows that unconditional stability is achieved at the whole swept frequency range.

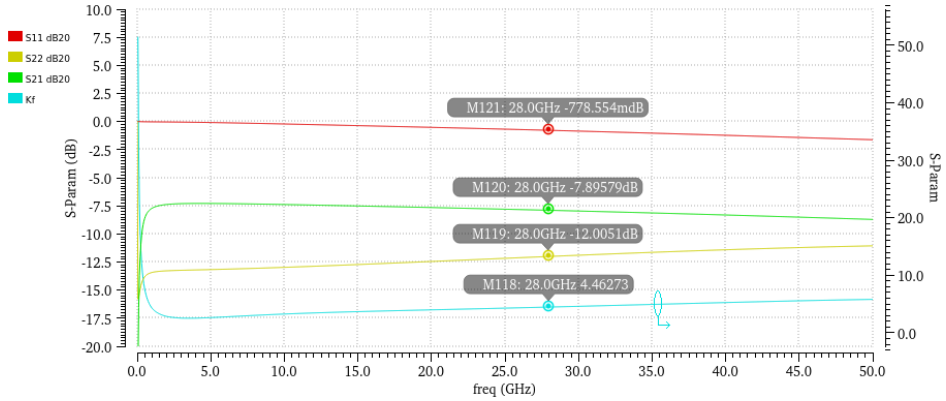

Figure 27. S-parameters as a function of frequency.

The S-parameters S_{11} and S_{22} are desired to be under 0 dB. S_{11} marked with M121 shows the value of -0.78 dB and M119 shows a value of -12.0 dB for S_{22}. Especially the S_{22} shows a really good value for the reflection of the output side of the circuit. The parameter S_{21} shows -7.90 dB, meaning that the circuit has forward voltage attenuation. This is not to be mixed with the power gain of the circuit presented earlier. S-parameter simulations showcase forward and reverse voltage waves, thus the gain presented by S-parameters is voltage gain. [34][35]

5.2.3 Harmonic balance simulations

5.2.3.1 Input power sweep

When designing the expansive behaviour for the circuit, the input power sweep shows the gain characteristics needed. With the expansive gain, the linearizer gives more room for linear operation of the main amplifier device. The main goal was not to get gain out of the expansive linearizer but to push the compression point of a PA further. The advantage of this design is the controllability to change the amount of expansion. This change is nothing drastic, but it gives some room to balance between expansion and gain.

First of all, Figure 28 shows the expansive behaviour of the design. The gain of the design is 312 mdB at low input power and it starts to expand around -20 dBm of P_{IN} and rises to 3.22 dB. This gives the circuit expansion of 2.91 dB with gate biases of 185.5 mV for PMOS and 611.6 mV for NMOS. 1dB compression point of the circuit is -4.54 dBm.

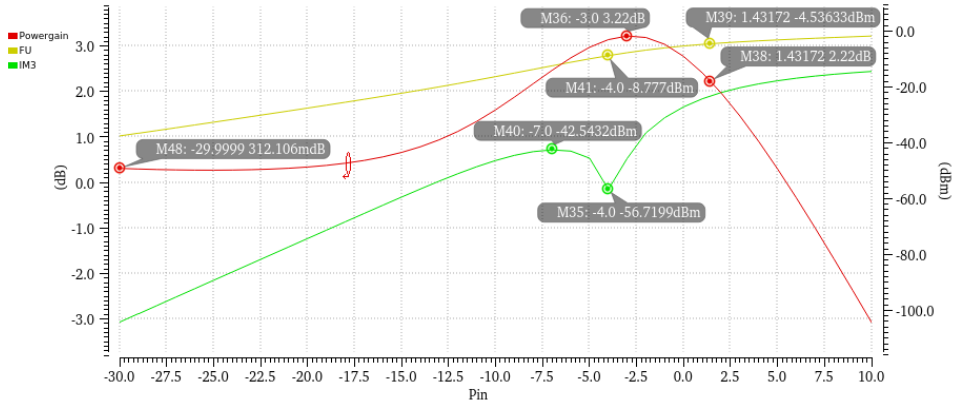

Figure 28. The gain, fundamental and IM_3 curves of the complementary design as a function of input power.

At a P_{IN} of -4 dBm, there is a sweet spot for IM_3 giving an improvement of over 14 dB when markers M35 and M40 are compared. The IM_3 sweet spot occurs where the signal starts to compress. At this point, the design has certain components of IM_3 at opposite phases and thus cancelling each other causing the IM_3 minimum to be a narrow dip, unlike in the conventional DS where the cancellation happens at a wide range of input amplitude. This kind of sweet spot behaviour of intermodulation distortion is described more thoroughly in [6 p. 74-77], [37] and [38].

The design gives possibilities to adjust the gain and expansion of the circuit with gate biasing. As can be seen from Figure 29, there is much room for variation. In the simulation presented, the biasing values are changed with DAC control variables. The control variable K1 sets the biasing of the auxiliary PMOS transistor and the K2 variable sets the biasing of the main NMOS transistor. Table 1 presents the K-values with their corresponding voltage biases used to simulate the results in Figure 29. With more K-values, there are even more combinations for different gain-expansion curves.

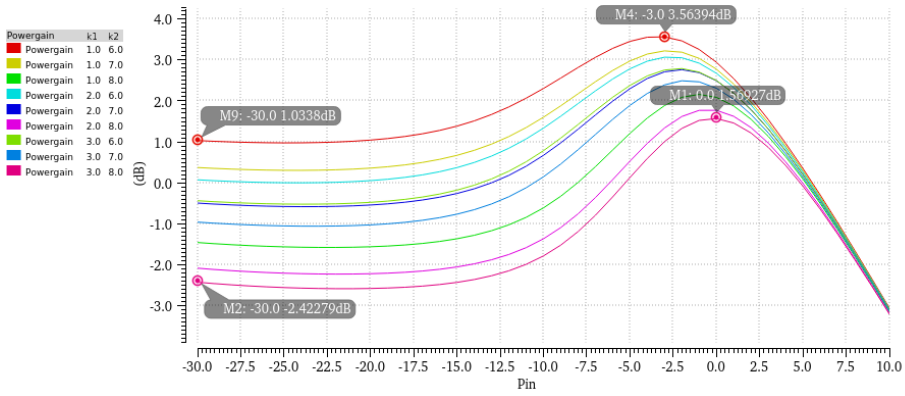

Figure 29. The gain variation of the design with different gate biases.

Table 1. Bias voltages respect to K-values (K1 and K2 are the bias voltages set for the PMOS and NMOS devices, respectively)

K1		**K2**	
1	185.5 mV	6	611.6 mV
2	212.3 mV	7	628.3 mV
3	227.7 mV	8	653.1 mV

Table 2 presents low drive gain, maximum gain, and expansion for all the curves in Figure 29. From these results can be seen, that the gain level gets lower when each bias is increased. When the main transistors biasing point is increased, the gain drops due to the DC voltage at the drain. When the transistor starts to conduct more, the DC voltage at the drain drops, thus lowering the gain, keeping the drain current almost the same. When increasing the biasing of the auxiliary device (PMOS), the DC current and drain voltage drops, thus lowering the gain.

Table 2. Comparison of all gains and expansions from curves of Figure 29

Curve	K1	K2	Gain (dB)	$Gain_{max}$ (dB)	Expansion (dB)
	1	6	1.03	3.56	2.53
	1	7	0.36	3.22	2.86
	1	8	-1.45	2.16	3.61
	2	6	0.08	3.07	2.99
	2	7	-0.49	2.76	3.25
	2	8	-2.08	1.77	3.85
	3	6	-0.43	2.16	2.59
	3	7	-0.96	2.49	3.45
	3	8	-2.42	1.57	3.99

When the input power gets high enough, the gain starts to expand and with lower gain, there is more room for the signal to expand before it starts to compress. With the lower gain, more expansion is thus achieved. This gives the linearizer adjustability to predistort the possible power amplifier. If the amplifier does not have room for a little attenuation in the gain, the linearizer can be adjusted to have no attenuation, but then has a lower expansion. If more expansion for the main amplifier is desired, the expansion can be tuned to be higher, with the cost of some attenuation, lowering the overall gain of the design yet improving the linearity.

5.2.3.2 Frequency sweep

The frequency sweep of the circuit shows some interesting results in Figure 30 and Figure 31. With the P_{IN} of -3 dBm, which is the point of maximum gain for the circuit, the IM_3 curve shows some variations over frequency in Figure 30. IM_3 curves show a local minimum at around 37.7 GHz. At 28 GHz, which is the desired operating frequency, the IM_3 (marker M8) and IM_5 (marker M7) output power levels are almost at the same level.

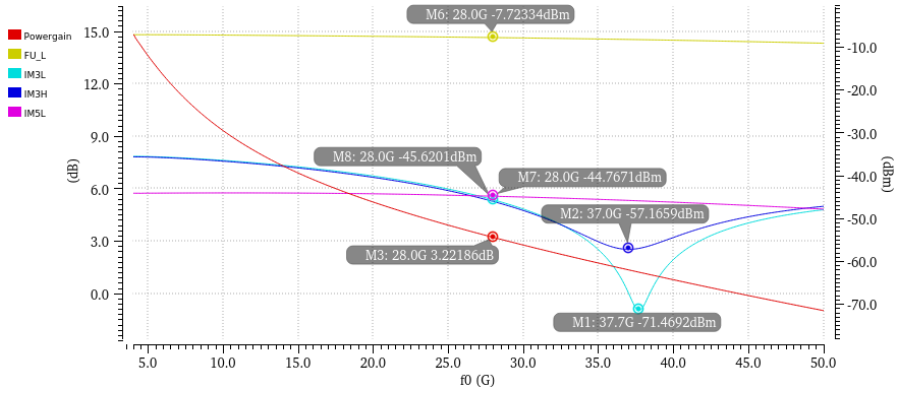

Figure 30. Power gain, lower fundamental, IM_3 low and high, and lower IM_5 as a function of frequency with a P_{IN} of –3 dBm.

In Figure 31 is presented the same simulation as in Figure 30, but with a different input power of -4 dBm, which is the sweet spot for the IM_3 output power.

In Figure 31, the IM_3 has its lowest point at a frequency of around 24 GHz. When compared to Figure 30, where the lowest point of the same tone is at around 37.7 GHz, it is seen that the place of the IM_3 sweet spot is dependent on the input power and with steady input power, the IM_3 level is dependent on the frequency. The minimum is moving and varying when the biasing

is varying with different input power level. When sweeping the input power, the IM_3 level is seen only at one input frequency. Around P_{IN} of -4 dBm, the input power dependant sweet spot moves closer to the observed frequency of 28 GHz, thus showing the result, and sweet spot, as is seen in Figure 28.

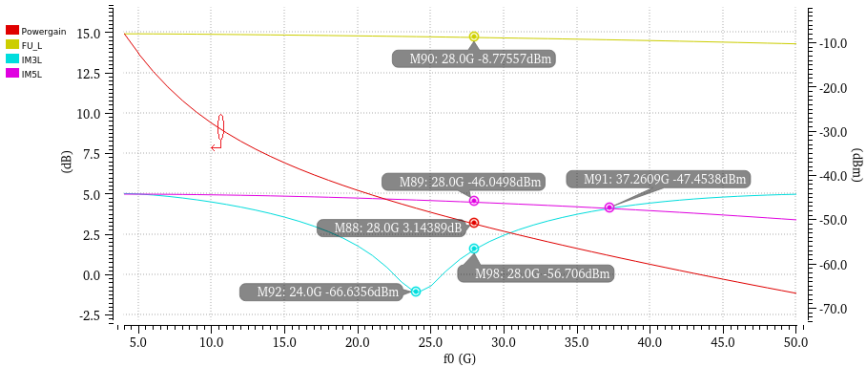

Figure 31. Power gain, fundamental, IM_3 and IM_5 as a function of frequency with a P_{IN} of -4 dBm.

At lower frequencies than 37.3 GHz, marked with M91, the IM_5 level is higher than the IM_3. For this circuit, the intermodulation product power levels were not the main point of interest, so that is not something of a huge issue at this stage.

When the two figures are compared, the varying input power only affects the sweet spot of the IM_3. Other curves, such as gain and fundamental keep their shape, only with a little of a variation in the level coming from different input power level and expansive behaviour.

Because the circuit has an inductor and a capacitor at the source of the PMOS transistor, as shown in Figure 9, they cause resonance to a certain frequency. This could have been an issue, but the components were designed to have the resonance at a much higher frequency than the 28 GHz, thus not affecting the gain. The resonance frequency can be calculated as

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{9}$$

where f_r is the resonance frequency of the LC-circuit, L is inductance and C capacitance. For layout size reasons, the inductor size was dimensioned first. To achieve a small layout for the circuit and inductor being the most space taking individual component, the physically smallest possible inductor for the technology used was chosen. The used inductor has an inductance of 111.1 pH. For the bypass capacitor, it was also possible to use a physically small capacitor, which then gives a small capacitance, thus making the resonance frequency to be higher. With a capacitance of 6.1 fF, which is almost the smallest available capacitance, the resonance frequency is at 193.6 GHz. Figure 31 shows, that at least up to 50 GHz of the simulated band, the resonance frequency is not affecting the gain.

5.2.3.3 Tone spacing

The tone spacing simulation of the circuit reveals some memory effect. With a centre frequency of 28 GHz and input power of -3dBm, the tone spacing sweep in Figure 32 confirms the variance over swept tone spacing. With a narrow tone spacing, all the IM tones are around -37 dBm, but as the spacing widens, the IM_3 levels experience a decrease to around -50 dBm before

settling to around -45 dBm. Fortunately, all the simulated IM tones have a lower level with a wider tone spacing, thus causing no issues. The simulation also confirms the result from Section 5.2.3.2, that the IM_5 level stays higher than the IM_3 over the whole swept tone.

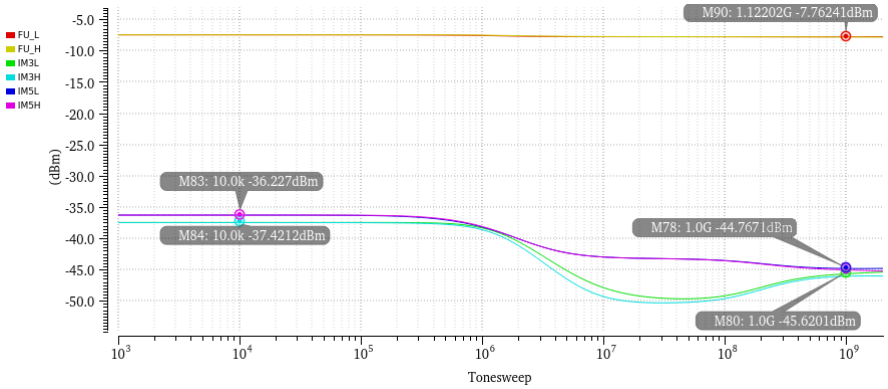

Figure 32. Fundamental, IM_3 and IM_5 lower and higher tones as a function of tone spacing.

5.2.4 Transient analysis

Figure 33 is showing the transient analysis simulation results of the circuit with the same test setup and input pulse as in 5.1.5. The simulations showcase similar results as earlier. The only difference is the amount of the numerical values of the output voltage. The voltage keeps bouncing very sharply with a change of 17.5 µV and an exact time difference of 2 ns. There is also a small amount of offset which is slowly steadying towards zero. No ringing or instability can be seen in the simulation.

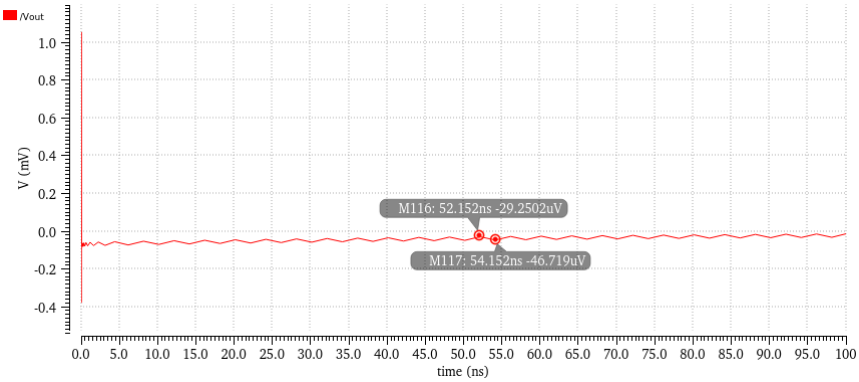

Figure 33. Transient analysis showing output voltage as a function of time.

5.2.5 The effect of parasitic extraction

The parasitic extraction also affects this circuit. The effect of the attenuation is clearer at a higher level of gain as can be seen in Figure 34. At the lowest input power swept, the effect of parasitic extraction is 148 mdB, but when moved to higher input power, the gain does not expand as much. The highest peak of gain moves to lower input power and the maximum gain is 0.94 dB lower. The parasitic extraction has also affected the IM_3 curve, shifting the place of the local minimum to lower input power caused by the gain starting to compress earlier.

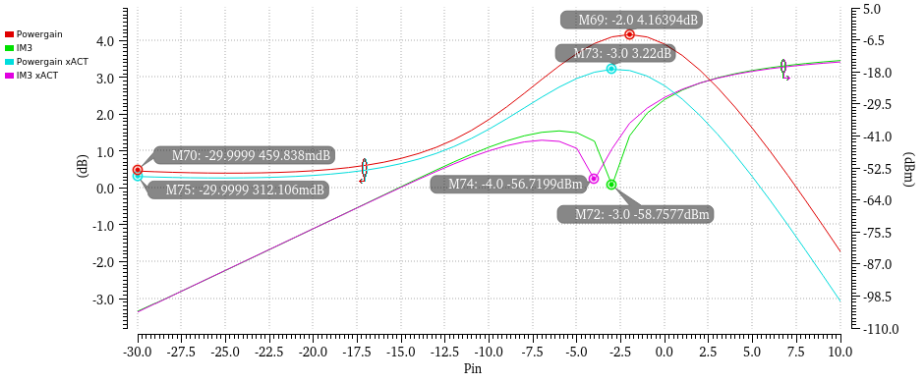

Figure 34. Comparison of gain and IM_3 with and without parasitic extraction as a function of input power.

5.3 Simulation summary

Table 3 presents all the most important measurement results gathered from the simulations. Because of the different aim of the operation, some notes are added to explain the results.

Table 3. Summary of simulation results

	Conventional	**Complementary**	**Notes**
DC-current	4.68 mA	4.52 mA	DAC currents are not included
Gain	8.87 dB	0.31 dB	Complementary DS gain and expansion are adjustable
$Gain_{max}$	8.87 dB	3.22 dB	
Expansion	-	2.91 dB	No expansion in Conventional DS
P1dB	-6.51 dBm	-4.54 dBm	
IM_3 improvement	25.8 dB	(14 dB)	Complementary improvement only at narrow drop
Sweet spot location (at P_{IN})	-16 dBm	-4 dBm (-3dm)	-4dBm for IM_3 -3dBm for expansion
S_{11} (@1 GHz)	-0.80 dB	-0.78 dB	
S_{22} (@1 GHz)	-1.52 dB	-12.01 dB	
S_{21} (@1 GHz)	0.65 dB	-7.90 dB	
K_f (@1 GHz)	0.5	4.46	
Layout dimensions (Width x Height)	22.9 µm x 17.1 µm	54 µm x 118.4 µm (13.4 µm x 34.4 µm)	In brackets the size without inductor

6 LINEARIZATION OF POWER AMPLIFIER

Section 6.1 presents the simulation results of the conventional DS circuit combined with a CMOS power amplifier. In Section 6.2 the complementary DS structure presents the effect of expansive linearization with the same CMOS power amplifier.

6.1 Distortion cancellation

The conventional derivative superposition circuit was simulated with the CMOS power amplifier to see the effect of the linearization. Figure 35 illustrates three amplifier setups used for the simulations. First, case a) uses the linearizing circuit as a predistorter in front of the PA marked as LIN. Second, case b) has a comparison setup with a preamplifier. The PA is amplified with a nonlinearized preamplifier with a similar gain to the linearizer to review the effect of less linear preamplification on the distortion level in the output of the power amplifier. The third setup, c), has the PA individually so the power amplifiers gain by itself can be simulated. The outputs of the linearizer and preamplifier are taken from the nodes between them and the power amplifier. These simulations do not have the PEX results included for the circuits.

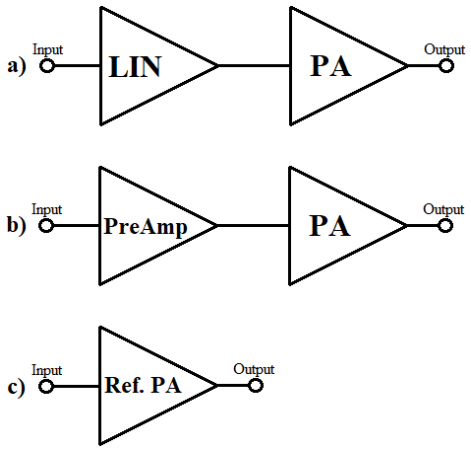

Figure 35. Simulation setups used in linearization performance simulations using conventional DS circuit and CMOS PA.

The gains of the three simulation setups are represented in Figure 36. The green curve shows the gain of the reference power amplifier. It has a gain of 17.4 dB. Red and yellow curves illustrate the gains of a) and b) in Figure 35, respectively. The preamplifier created for this simulation was set to provide a similar gain as the predistorter. This can be seen in Figure 36, as the red and yellow curve have just over 0.5 dB difference in the gain. The gains are 34.7 dB and 34.1 dB for linearized PA and comparison PA, respectively.

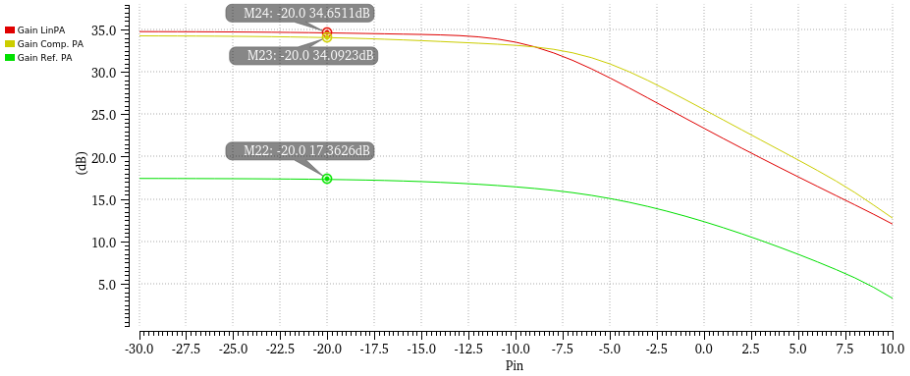

Figure 36. Power gains of linearized power amplifier, preamplified power amplifier and reference power amplifier.

Figure 37 reveals that both pre-circuits push the P1dB point higher. The P1dB of the reference PA is 5.96 dBm whereas the preamplified PA P1dB is 6.42 dBm and the linearized PA P1dB is 8.56 dBm. Even though the linearized was not meant to provide that much gain linearization, the P1dB was pushed 2.6 dB higher while also pushing it over 2 dB higher than the simple preamplifier.

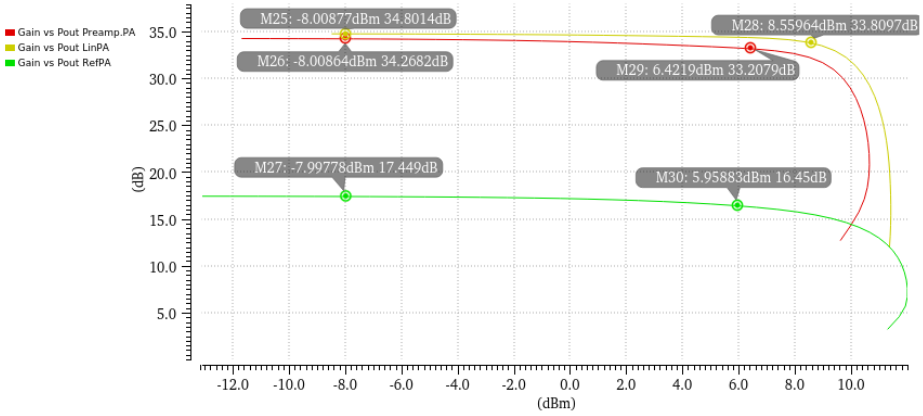

Figure 37. Gains of the preamplified PA, linearized PA and reference PA as a function of fundamental output power.

Figure 38 presents the IM_3 levels of all three power amplifier outputs as well as predistorter and preamplifier outputs. When the preamplifier and predistorter are compared, the cancellation effect can be seen. The predistorter has a lower IM_3 level with low input but it has worse performance with high input. What comes to the cancellation, with the PA the load differs from the ideal load of 50 Ω, causing the cancellation behaviour to change. The biases of the conventional derivative superposition circuit needed some adjusting and as good cancellation as with the 50 Ω load was not achieved.

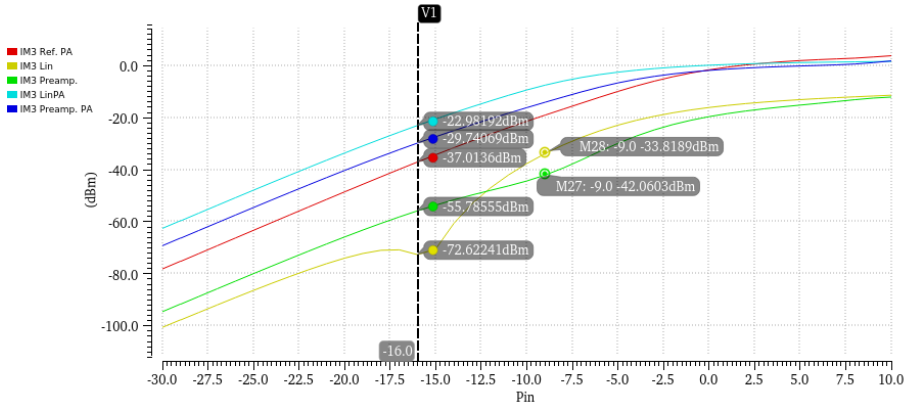

Figure 38. IM_3 levels of the simulated amplifier circuits.

The PA circuits have similar IM_3 performance with low input. At P_{IN} of -16 dBm, the linearized PA has the worst IM_3 performance with preamplified PA coming second. As the IM_3 performances are reviewed as a function of the input power, the complete truth about the distortion performance is not seen. All the circuits do have the same input power, but as they have a different amount of gain, the output levels differ, which causes the IM_3 levels not to be completely comparable.

Figure 39 presents the output IM_3 power with corresponding fundamental output power. This gives a better estimation of the IM_3 performance when different circuits are compared. As can be seen, the reference amplifier presented with a yellow curve still has the lowest distortion level, since it does not have any driver in front of it that is already distorting the input signal. What comes to the linearized and preamplified circuits, the performances are opposite than in Figure 38. The linearized PA output is 2.9 to 2.5 dB better from -7 to 0 dBm of fundamental output power. However, no significant amount of improvement in the distortion level caused by the cancellation can be seen. The effect of cancellation causes the linearizer to add less distortion to the power amplifiers distortion, but it does not cancel it, which is quite obvious.

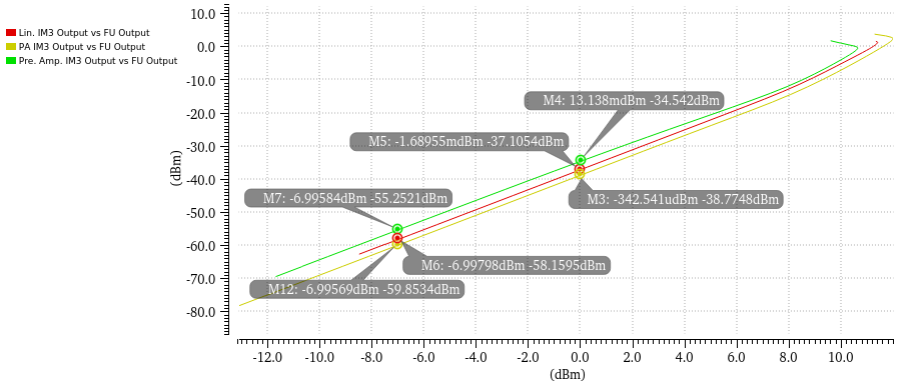

Figure 39. The output IM_3 powers as a function of output fundamental powers.

When the three cases are compared in dBc, the results are different. The dBc value describes the relation of the IM_3 and the fundamental signal. The dBc value is higher when the IM_3 is lower compared to the fundamental. In Figure 40 the dBc value is the highest for the reference PA (green) itself, followed by the preamplified PA (yellow) leaving the linearized PA (red) to be the lowest. The reference PA itself having the highest level can be explained via the IM_3 levels 3dB/1dB relation to the fundamental. The reference PA has the lowest gain and thus lowest fundamental, so the IM_3 level is three times as low. Comparison between the reference

PA and linearized PA state that the proposed predistorter design seems not to be an optimal solution as an individual predistorter. It does not provide predistorter power for cancellation and is not that good solution as a linear preamplifier from an IM_3 perspective.

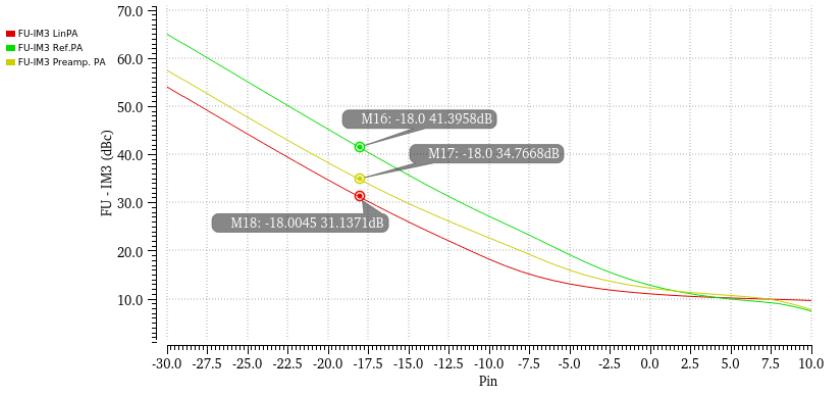

Figure 40. IM_3L level in dBc as a function of input power.

Next, we study how the conventional DS circuit affects the AM-PM of the PA. Figure 41 illustrates the phases of the reference PA, linearized PA and comparison PA. The reference power amplifier phase rises from 37 degrees to 55 degrees. This is not critical, as the phase is flat at the amplifiers dynamic range. The preamplifiers do cause a little variation to the phase at under -5 dBm of a P_{IN} but nothing more than 5 degrees. The variation is smaller with higher input power which is, unfortunately, irrelevant because the used PA is not usable with such high input power.

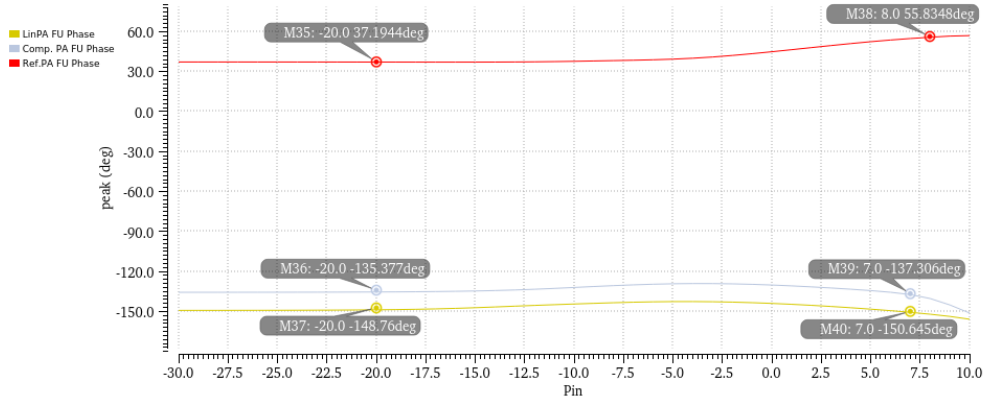

Figure 41. Simulated fundamental phases of the amplifier circuits.

In conclusion, the conventional derivative superposition circuit is working rather as a linear preamplifier than a predistorter. It provides additional gain and improves power amplifiers 1 dB compression point while keeping the IM_3 level at a reasonable level. The effect of IM_3 improvement cannot be seen clearly at the output of the PA but it lowers the additional distortion coming into the power amplifier, thus providing slight improvement.

6.2 Expansive linearization

The complementary derivative superposition circuit was simulated with a power amplifier, as is presented in Figure 42. The simulation setup a) has the linearizer in front of the power

amplifier to simulate the effect of the expansion to the output of the power amplifier and the simulation setup b) has the reference PA individually to simulate the original output. The output of the linearizer is taken from the node between the linearizer and power amplifier.

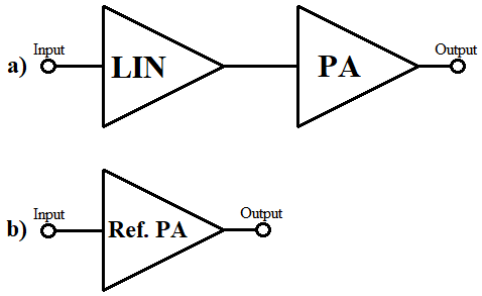

Figure 42. Simulation setups for the expansive linearizer and CMOS PA.

The used power amplifier was first biased to have maximum gain causing the output to start compress earlier. The nonlinearity was then compensated by biasing the linearizer accordingly. Figure 43 illustrates all the gains as a function of input power. In addition, Figure 44 represents the gain as a function of fundamental output power from where the P1dB can be seen. The yellow curve in Figure 43 presents the gain of the used power amplifier. The gain of the reference amplifier is 20.7 dB with a P1dB of 5.32 dBm.

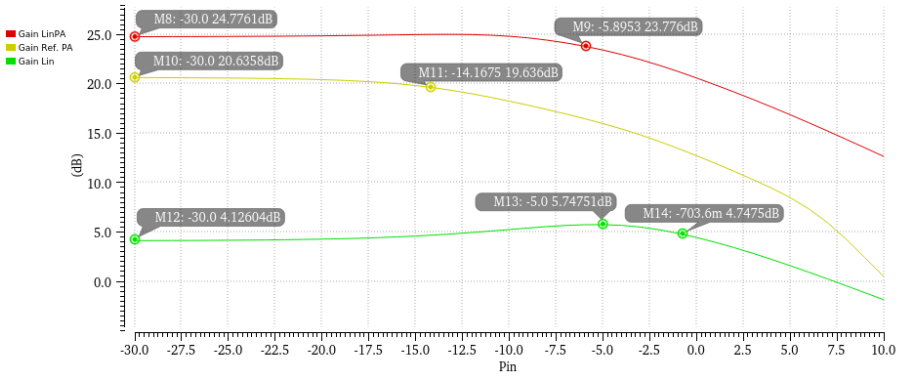

Figure 43. The gains of proposed linearizer design, power amplifier and both combined.

The expansive linearizer was biased to achieve a certain amount of expansion so that the PA output was as linear as possible. The expansion was tuned down by setting gate biases to 185.5 mV (K1 = 1) and 568.5 mV (K2 = 4) for the PMOS and NMOS, respectively. With these biases, the linearizing circuit, green curve, has a gain of 4.1 dB with an expansion of 1.6 dB.

The red curve in Figure 43 presents the linearized power amplifier gain. The gain of the linearized structure is 24.8 dB and the P1dB is 8.82 dBm as can be seen from Figure 44. The compression point was achieved to be 3.51 dBm higher.

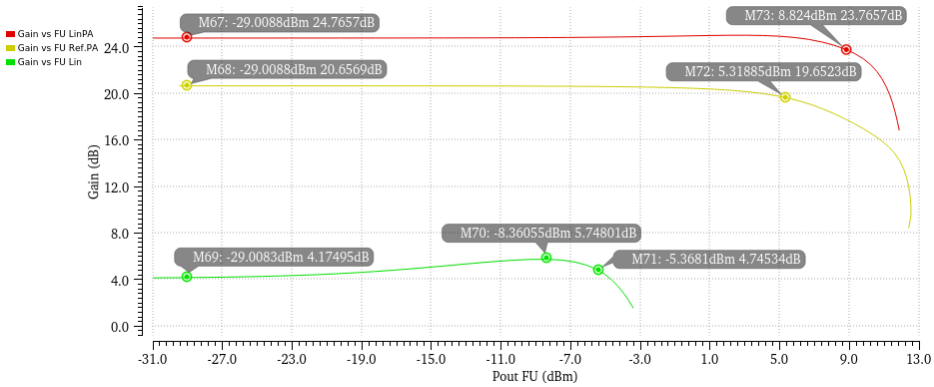

Figure 44. Gains of linearized power amplifier (red), reference power amplifier (yellow) and linearizing circuit (green) as a function of fundamental output power.

The IM_3 power as a function of output power for the circuits is presented in Figure 45. Green, yellow and red curves present linearizer, reference PA and linearized PA, respectively. The linearizers individual IM_3 performance is much worse than the other two curves. Nevertheless, when the reference PA and linearized PA are compared, the IM_3 performance of the linearized PA is only a little bit worse, with a difference of 3.3 dB.

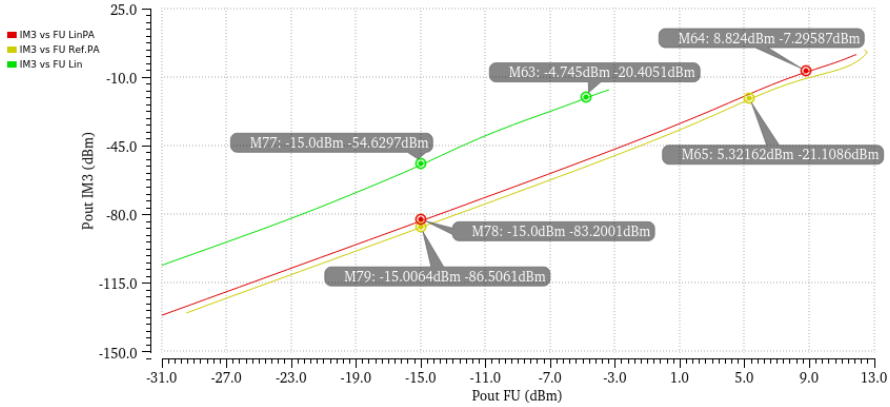

Figure 45. IM_3 output power as a function of fundamental output power.

The expansive linearizer on its own is a highly nonlinear circuit. When combined with a power amplifier with the opposite nonlinearities, the linearity gets better, which then causes the distortion level to improve.

Even further comparison to the IM_3 level of the linearized PA and reference PA can be simulated. As can be seen in Figure 46 the dBc value is higher for the linearized PA, implementing that the linearity is improved. The assumption was, that the dBc value for the linearized PA stays better to higher power levels as the reference PA achieves saturation earlier. However, the reference PA has a region at the higher input where the dBc value is better. This happens just before the linearized PA reaches its P1dB. Still, the linearized PA performs better almost at the whole dynamic region.

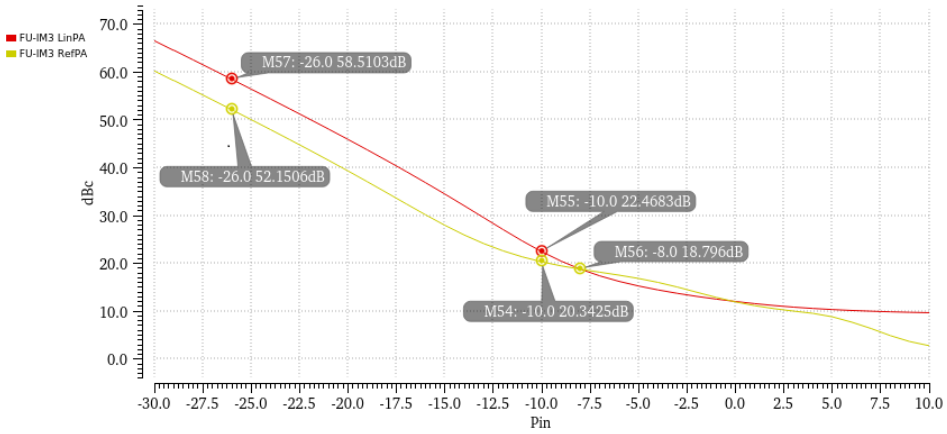

Figure 46. IM_3L level in dBc as a function of input power.

The fundamental phase correction of the linearizer is seen with high input power, outside of the dynamic region of the amplifier. In Figure 47 it is seen, that the overall phase modulation is improved, mainly after the amplifier has reached saturation. But as the amplifier has such a flat phase at the operation range, the main thing is that the linearizer does not worsen the phase of the amplifier at the dynamic range area.

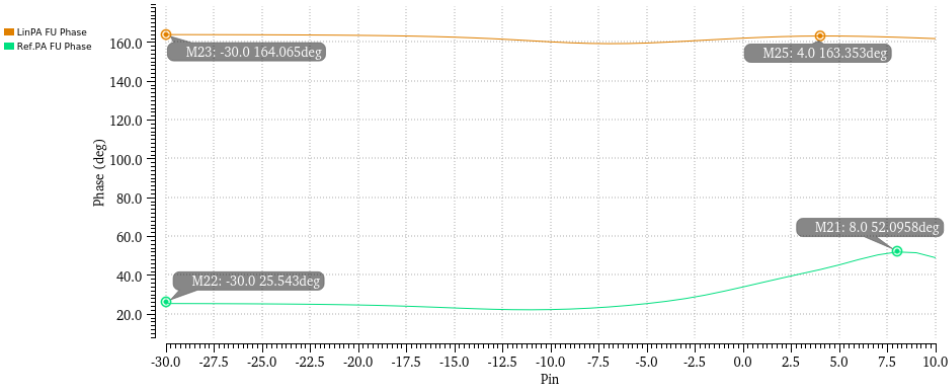

Figure 47. Power amplifier phase with (orange) and without (green) linearization.

Figure 47 somewhat proves the fact, that by correcting the nonlinearity in the amplifier, the distortion is not the only thing that gets better. There are multiple things to be considered, phase being one of them. The desired quality of a power amplifier is to have the phase curve as flat as possible.

In conclusion, the predistorter with expansive gain performs with a power amplifier as it was designed to. The P1dB was pushed further to give the amplifier a more dynamic range thus providing better efficiency. The distortion level does not rise too much, even though it was not the main focus when this linearizing circuit was designed. In addition, the phase modulation of the amplifier flattens with the linearizer.

7 DISCUSSION

The goal was to improve the distortion level of the signal, with solutions using expansion and distortion cancellation for linearisation. By using these two different linearizing solutions, two different circuits were successfully designed with pre-set qualities.

With the conventional derivative superposition circuit, a fair amount of cancellation of the intermodulation distortion was achieved. This meant the improvement of over 25 dB in the distortion level.

In the complementary derivative superposition, the desired quality of expansive behaviour was achieved with the additional capability to adjust the amount of expansion. This gives room to adjust the predistorter to fit the power amplifiers qualities. Easy adjustability is a good feature to have, so that the circuit is easier to implement, without the need of changing the transistors or components sizes.

With a power amplifier, the results were confirmed further. The conventional derivative superposition circuit worked as a linear preamplifier. The cancelling effect did not work with the power amplifier as good as would have been ideal. The cancellation in the predistorter could not be seen clearly at the output of PA and when compared to a simple preamplifier, the results were not as good as wanted. Nevertheless, it improved the P1dB point of the power amplifier over 2.6 dB while providing a fair amount of gain. The output distortion of the PA as a function of fundamental output power was around 3 dB lower with the conventional DS as a preamplifier. To improve the distortion of the power amplifier, a similar two parallel transistors setup could be used inside a power amplifier. The two parallel transistors would replace one transistor in the amplifier, thus causing cancellation inside the amplifier. This could improve the amplifiers IM_3 performance.

The predistorter with expansive gain linearized the amplifier just as wanted. The gain and expansion were adjusted to match the compression of the power amplifier. This verified the adjustability of the circuit and provided the results desired. The output got more linear and the compression point was pushed 3.5 dBm further. With a higher compression point, the power amplifier can work with better efficiency and the dynamic range of the power amplifier becomes wider.

With more time, this thesis could have been improved by having measurement results of the circuits. At this given time, the circuits were under fabrication, so the measurement results for this thesis were not available. This could have given the thesis a little more versatility when the broad simulation results could have been compared with the measurement results of the real circuit. Some parts of the design were made considering future measurements. The transistor back-gates were enabled so that there would be more parameters to change to find optimal measurement values for the designs. Especially, the conventional derivative superposition can be biased to cancellation using either or both biasing methods. As it was presented in this thesis, these biasing methods should not have much of a difference, but in reality, there might be more of a difference.

An additional point of interest in the measurements to be done is in the complementary derivative superposition circuit. The input dependant minimum seen is an interesting effect. The root cause of the minimum could be examined more. It is not clear where it comes from. Because it is input dependant, it could be the change in input capacitors that is causing it, since the response of the capacitors is frequency-dependent. When the bias changes it might cause a change in the resonance frequency. However, a similar effect cannot be seen in the other design, so it cannot be completely caused by the capacitors. Furthermore, the effect is completely in

the 3rd-order intermodulation distortion when usually the resonance has also effect on the fundamental.

Without measuring the manufactured circuit, there is no full proof that the design flow was completely successfully implemented. Even though the broad variety of simulations give a good estimation that the circuit works as it is intended, there might still be errors in the layout or the components. Such error might be in the capacitor used as a bypass capacitor in the conventional derivative superposition circuit. The capacitor has a maximum voltage of 1.8 V, which should be enough, considering the used supply voltage is 800 mV. There is still a slight concern of peaks, thus the better solution would have been to use a capacitor that can handle more voltage over it. Of course, the different capacitor would have different properties, thus needing some adjusting. This concern, for example, cannot be seen in simulations and if the capacitor has a voltage breakdown, it might break the whole circuit.

To examine the results further, different transistor types could have been used. The only transistor type used and implemented in this thesis was the SLVT transistors. To examine the operation and results of different threshold voltage transistors could have given more understanding of more suitable transistor implementations and their contribution to the currents and gains. Another simulation that would have given a broader result base would have been the simulations with different conditions. These simulations were done using normal conditions without, for example, worst-case scenarios, where the temperature affects the operation. Additionally, to simulate real conditions, an extensive electromagnetic simulation could be performed, to inspect the electromagnetic effect on the operation of the circuit, as well as non-ideal grounds, could have been used. The non-ideal grounds were not used, as the assumption was, that there is no significant change in the properties of the circuits, thus simple circuit modelling was used. The non-ideal grounds would have made a bigger difference with a higher frequency.

To push the predistorters even further in the future, some phase adjustment could be added. With phase adjustment, the predistorters distortion can be rotated to work with the power amplifier similarly as the distortion works in conventional DS design at the transistor level. The phases would be adjusted to be the opposite, thus cancelling the distortion further. At this stage, the designed circuits do not have this capability.

8 SUMMARY

Two simple integrated predistorters were designed to be as a part of MIMO transceiver implementation to linearize the power amplifier and thus the distortion of the whole design would improve. The circuits were implemented using 22 nm CMOS FDSOI technology. These two predistorters provide two different solutions to improve the distortion.

Amongst circuit designs, the theory of the individual circuits, as well as schematics, were presented. With a conventional derivative circuit, the distortion level is improved with cancellation. This means that two parallel NMOS transistors are biased to have IM_3 components to be different signs, thus cancelling each other. With this kind of design, more than 25 dB improvement was achieved in simulations. In complementary superposition structure, PMOS and NMOS transistors were used to achieve expansive gain. The design created was not biased to cancel the distortion as this type of structure would normally be, instead, it was used to achieve expansion. With this circuit, adjustable expansion and gain were achieved.

Layout design with measurement capability implementation was included in this thesis, as it is a crucial part of the design flow. Designs were made to work as individuals under one big layout structure with probing pads for the measurements. Some concepts used in layout design were introduced as they affect the layout design and results. Also, the measurement setup to be used in the future was briefly introduced.

The simulation part of this thesis covered a broad variety of different simulations to cover the operation of both circuits. Simulations presented the wanted distortion improvement for the conventional derivative superposition design by improving the 3rd-order intermodulation distortion by over 25 dB. Complementary derivative superposition circuit achieved adjustable gain and expansion behaviour. The expansion was simulated to be adjustable at least from 2.5 dB to 4.0 dB, with a possibility of even wider range.

Both of the circuits were simulated with a CMOS power amplifier, to verify if the circuits provided wanted improvements to the amplifier. The conventional derivative superposition circuit seemed to work as a linear preamplifier. The IM_3 improvement could not be seen clearly at the power amplifiers output but when it was compared with a simple preamplifier, the distortion level at the output was lower. The power amplifiers IM_3 output as a function of fundamental output power with the linearizing circuit was 2 to 3 dB lower than with the preamplifier. Also, 2.6 dB improvement in P1dB was achieved. The predistorter circuit (complementary superposition circuit) with expansive gain provided just the results wanted. The predistorters expansion was adjusted to compensate the compression of the power amplifier, which verified the adjustability of the circuit. The linearizer provided additional gain and pushed the P1dB compression point 3.5 dB higher allowing the power amplifier to be used with better efficiency.

9 REFERENCES

[1] Vuolevi J. H. K. & Rahkonen T. (2003) Distortion in RF power amplifiers.

[2] Peng J., He S., Wang B., Dai Z. & Pang J. (2016) Digital Predistortion for Power Amplifier Based on Sparse Bayesian Learning. IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, no. 9, pp. 828-832.

[3] Mkadem F., Islam A. & Boumaiza S. (2016) Multi-Band Complexity-Reduced Generalized-Memory-Polynomial Power-Amplifier Digital Predistortion. IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 6, pp. 1763-1774.

[4] Zhao K., Zhang S., Ho Z., Zander O., Bolin T., Ying Z. & Pedersen G.F. (2018) Spherical Coverage Characterization of 5G Millimeter Wave User Equipment With 3GPP Specifications. IEEE Access. vol. 7, pp. 4442-4452

[5] Sahlli E., Ismail M., Nordin R. & Abdulah N. (2017) Beamforming techniques for massive MIMO systems in 5G: overview, classification, and trends for future research. Frontiers of Information Technology & Electronic Engineering. Vol. 18, pp. 753-772.

[6] Aikio J. P. (2007) Frequency domain model fitting and Volterra analysis implemented on top of harmonic balance simulation. Acta Universitatis Ouluensis. C, Technica 272. University of Oulu, Oulu.

[7] Katz A. (2001). Linearization: Reducing distortion in power amplifiers. IEEE Microwave Magazine, Vol. 2, no. 4, pp. 37 - 49.

[8] Aikio J. P. & Rahkonen T. (2005) Detailed distortion analysis technique based on simulated large-signal voltage and current spectra. IEEE Transactions on Microwave Theory and Techniques, Vol. 53, no. 10, pp. 3057-3066.

[9] Vuolevi J. H. K., Rahkonen T. & Manninen J. P. A. (2001) Measurement technique for characterizing memory effects in RF power amplifiers. IEEE Transactions on Microwave Theory and Techniques, vol. 49, no. 8, pp. 1383-1389.

[10] Sorace R., Reines R., Carlson N., Glasgow M., Novak T. & Conte K. (2004) AM/PM distortion in nonlinear circuits. In: IEEE 60th Vehicular Technology Conference, September 26-29, Los Angeles, CA, Vol. 6. pp. 3994-3996

[11] Huang S., Xu Z. & Sun Z. (2014) Optimal input power back-off with nonlinear power amplifier for electric power systems. In IEEE International Conference on Communication Problem-solving, December 5-7, Beijing, China, pp. 5-8.

[12] Lavrador P. M., Cunha T. R., Cabral P. M. and Pedro J. (2010) The Linearity-Efficiency Compromise. IEEE Microwave Magazine, vol. 11, no. 5, pp. 44-58.

[13] Katz A., Wood J. & Chokola D. (2016) The Evolution of PA Linearization: From Classic Feedforward and Feedback Through Analog and Digital Predistortion. IEEE Microwave Magazine, vol. 17, no. 2, pp. 32-40.

[14] Nojima T. & Konno T. (1985) Cuber Predistortion Linearizer for Relay Equipment in 800 MHz Band Land Mobile Telephone System. IEEE Transactions on Vehicular Technology. Vol. 34, no. 4, pp. 169-177.

[15] Katz A., Gray R. & Dorval R. (2009) Truly Wideband Linearization. IEEE Microwave Magazine, vol. 10, no. 7, pp. 20-27.

[16] Jeong H. T, Chang I. S. & Kim, C. D. (2006) Compensation method for a nonlinear amplifier using the gain expansion phenomenon in a Doherty amplifier. IEEE Transactions on Microwave Theory and Techniques. Vol. 54, no. 4, pp. 1425-1430

[17] Aparin V. & Larson L. E. (2005) Modified derivative superposition method for linearizing FET low-noise amplifiers. IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 2, pp. 571-581.

[18] Sethi A., Rusanen J., Aikio J. P., Pärssinen A. & Rahkonen T. (2019) Broadband Linearization Technique for mmWave Circuits. In: 14th European Microwave Integrated Circuits Conference (EuMIC), September 30 – October 1, Paris, France, pp. 17-20.

[19] Zhang H. & Sánchez-Sinencio E. (2011) Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial. IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 58, no. 1, pp. 22-36.

[20] Sellier M. (2018) (Read 19.1.2021) FD-SOI: How Body Bias Creates Unique Differentiation. URL: https://www.globalfoundries.com/blog/fd-soi-how-body-bias-creates-unique-differentiation

[21] Vitale S. A., Wyatt P. W., Checka N., Kedzierski J. & Keast C. L. (2010). FDSOI Process Technology for Subthreshold-Operation Ultralow-Power Electronics. Proceedings of the IEEE, vol. 98, no. 2, pp. 333 - 342.

[22] Cheng K. G. & Khakifirooz A. (2016). Fully depleted SOI (FDSOI) technology. Science China Information Sciences, Vol. 59.

[23] Nguyen B., Flatresse P., Schaeffer J., Arnaud F. Mhira S., Huart V., Weber O., Sellier M & Maleville C. (2018) A Path to Energy Efficiency and Reliability for ICs: Fully Depleted Silicon-on-Insulator (FD-SOI) Devices Offer Many Advantages. IEEE Solid-State Circuits Magazine, vol. 10, no. 4, pp. 24-33.

[24] Olejarz P., Park K., MacNaughton S., Dokmeci M., & Sonkusale S. (2012). 0.5 µW Sub-Threshold Operational Transconductance Amplifiers Using 0.15 µm Fully Depleted Silicon-on-Insulator (FDSOI) Process. Journal of Low Power Electronics and Applications, Vol. 2, pp. 155-167.

[25] Schaeffer J. (2015) (Read 19.1.2021) 22FDX Platform, Enabling solution for IoT, Mobile, RF and Networking Applications. GlobalFoundries webinar. URL: https://www.gsaglobal.org/wp-content/uploads/2012/05/22FDX_GSA_AMS_Webinar_Schaeffer_rev2-JSA-rev-7.pdf

[26] Synopsys (Read 27.1.2021) What is Design Rule Checking? Synopsys website URL: https://www.synopsys.com/glossary/what-is-design-rule-checking.html

[27] Semiconductor Engineering (Read 27.1.2021) Design Rule Checking (DRC) URL: https://semiengineering.com/knowledge_centers/eda-design/verification/design-rule-checking-drc/

[28] Mentor Graphics Corporation (2006) (Read 27.1.2021) Calibre Verification User's Manual. URL: http://read.pudn.com/downloads218/ebook/1028073/calbr_ver_user.pdf

[29] Synopsys (Read 27.1.2021) What is Layout Versus Schematic Checking? Synopsys website URL: https://www.synopsys.com/glossary/what-is-layout-versus-schematic-checking.html

[30] Semiconductor Engineering (Read 27.1.2021) Layout Versus Schematic Checking (LVS) URL: https://semiengineering.com/knowledge_centers/eda-design/definitions/layout-versus-schematic-checking/

[31] Synopsys (Read 27.1.2021) What is Parasitic Extraction? Synopsys website URL: https://www.synopsys.com/glossary/what-is-parasitic-extraction.html

[32] Mentor Graphics corporation (Read 27.1.2021) Next-Generation Parasitic Extraction, Calibre xACT. Datasheet. URL:

https://s3.amazonaws.com/s3.mentor.com/public_documents/datasheet/products/ic_nanometer_design/calibre_xact-datasheet.pdf

[33] Kiuru V. (2020) RFIC piirin digitaaliohjaukseen vaadittavien piirirakenteiden suunnittelu. Master's Thesis. University of Oulu, Degree Programme in Electronics and Communications Engineering.

[34] Karris S. T. (2014) Engineering electromagnetics: with introductions to S-Parameters, RF Toolbox and SimRF., Appendix D.

[35] White J.F. (2004). Ensure stability in amplifier designs. Microwaves and Rf. Vol. 43, pp. 64-72.

[36] Rollett J. M., (1962) Stability and Power-Gain Invariants of Linear Twoports. IRE Transactions on Circuit Theory, vol. 9, no. 1, pp. 29-32.

[37] Carvalho N. B. & Pedro J. C. (2000). Large- and small-signal IMD behavior of microwave power amplifiers. , IEEE Transactions on Microwave Theory and Techniques. Vol. 47, no. 12. Pp. 2364 - 2374.

[38] Lee S.-Y., Jeon K., Lee Y.-S., Lee K.-S. & Jeong Y.-H. (2003). The IMD sweet spots varied with gate bias voltages and input powers in RF LDMOS power amplifier. In: 33rd European Microwave Conference, October 2-10, Munich, Germany, pp. 1353-1356.